SERVICE MANUAL & PARTS LIST (without price)

SF-8500(LX-575)

AUG. 1993

INDEX

CASIO®

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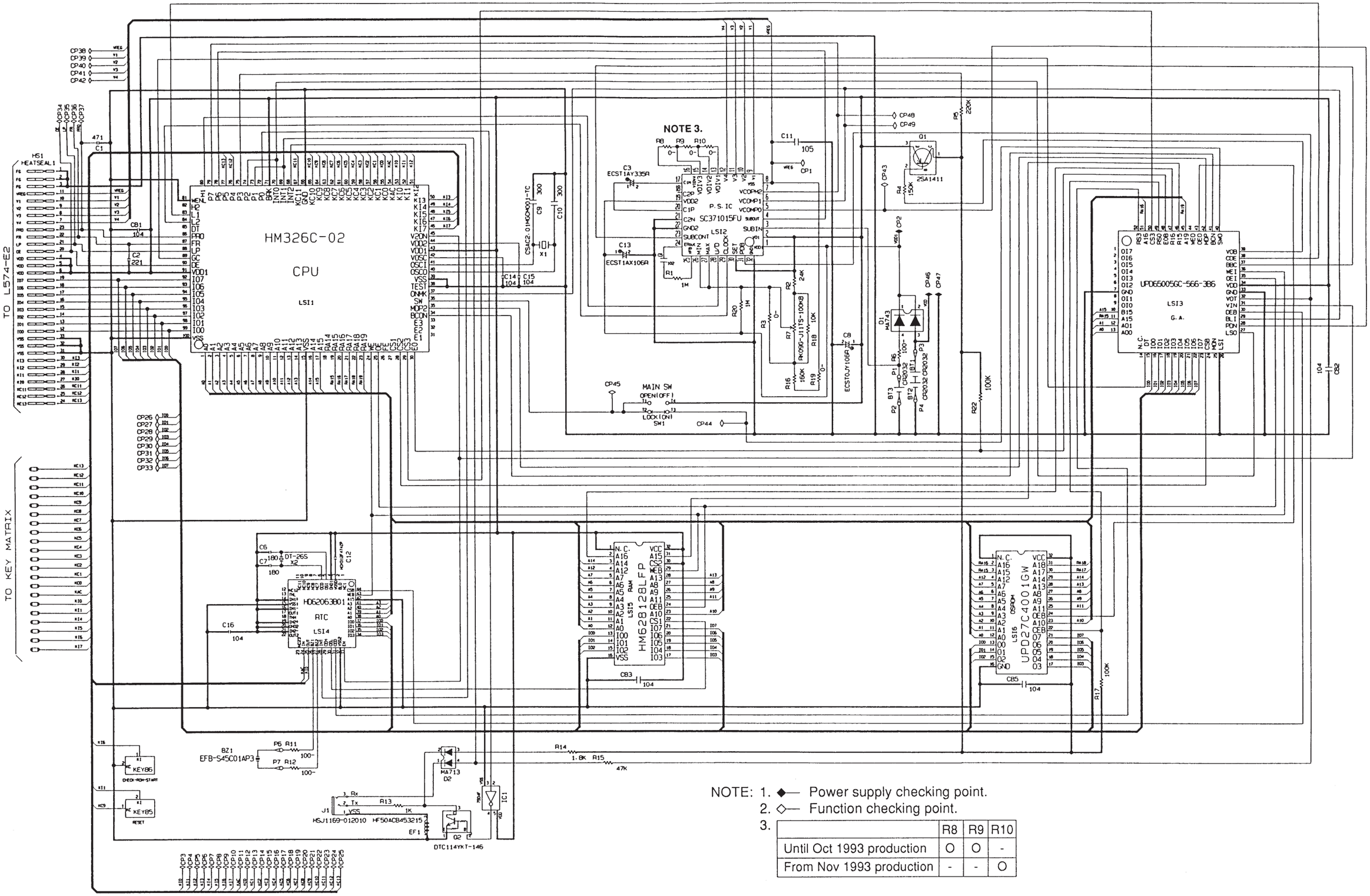
1. SCHEMATIC DIAGRAM

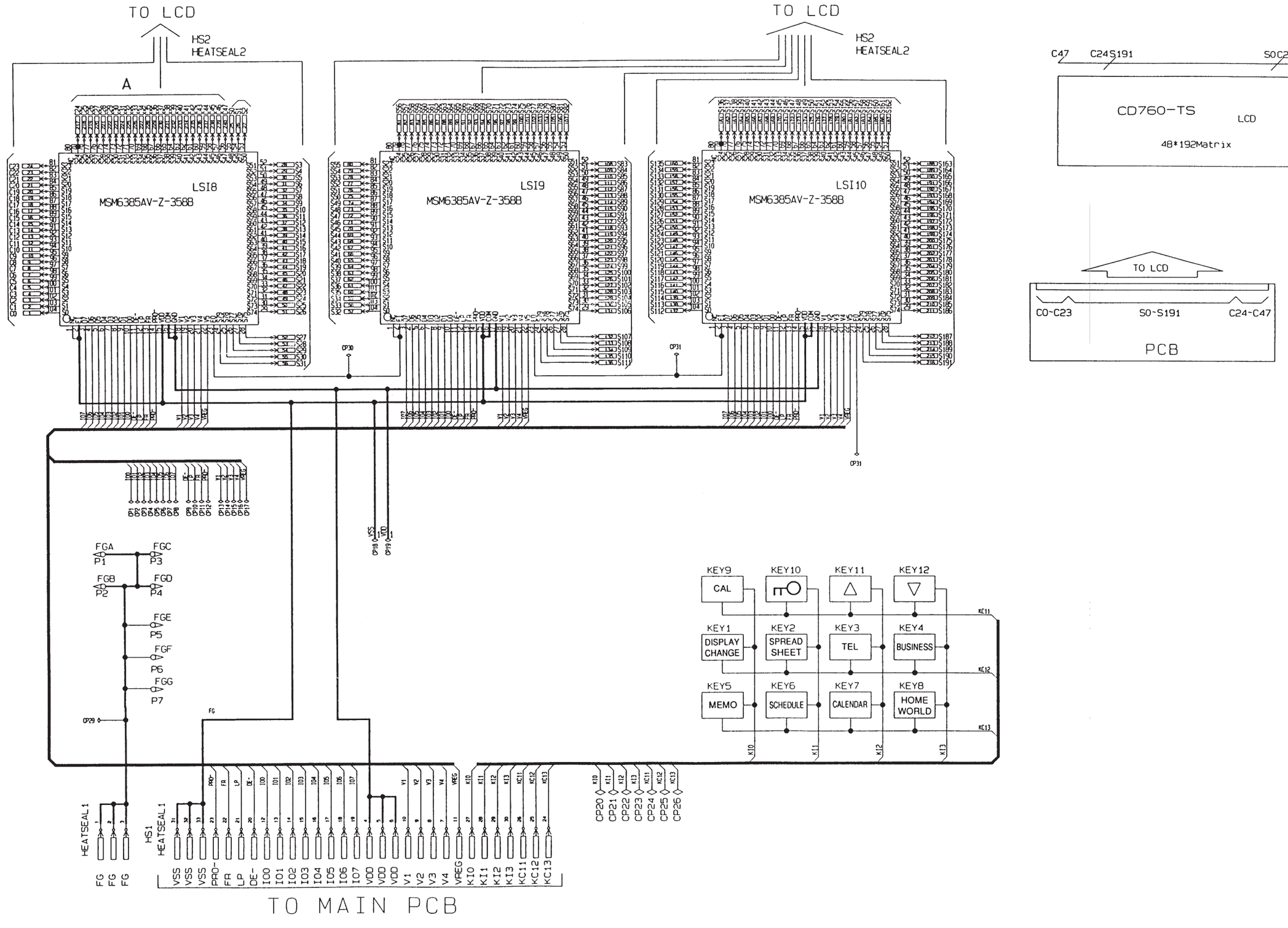
1-1. Main PCB

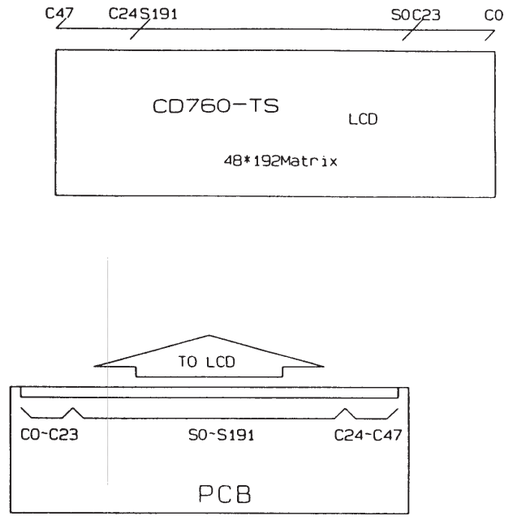


NOTE: 1. ◆— Power supply checking point.
2. ◇— Function checking point.
3.

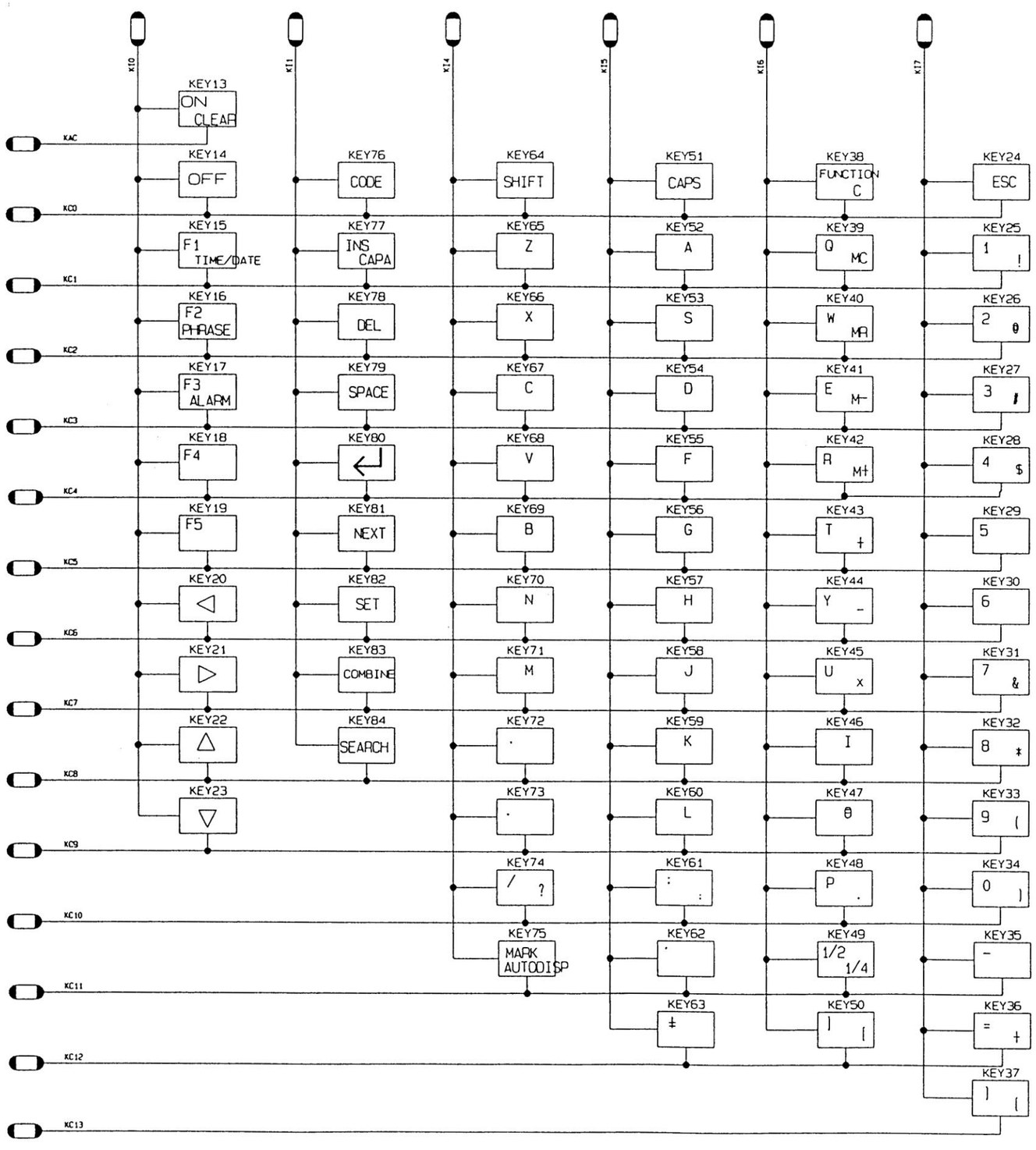
	R8	R9	R10
Until Oct 1993 production	O	O	-
From Nov 1993 production	-	-	O

1-2. Display PCB





1-3. Key Matrix



2. SPECIFICATIONS

Data storage:
Telephone/business card/memo/schedule data storage/recall, calendar display, marker, phrase memory, secret area, editing, capacity display, auto display

Clock:
Average of accuracy ±3 seconds per day under normal temperatures; worldtime, schedule alarm, daily alarm

Calculation:
12-digit arithmetic calculations, constants for +/–/×/÷, independent memory, percentages, square roots, 24-digit approximations, date calculations, other mixed calculations

General:

Display element:	32-column × 6-line LCD
Memory capacity:	64 KB (65,499 bytes) for the Spreadsheet Mode data plus 64 KB (51,910 bytes) for other mode's data
Main component:	LSI
Power supply:	Main Power Supply — Two CR2032 lithium batteries Backup Power Supply — One CR2032 lithium battery
Power consumption:	0.05W
Battery life:	Main: Approximately 120 hours (Repeated cycle of 1-minute data input into Telephone Directory followed by 10-minute display. Operation temperature of 20°C) Approximately 150 hours (Continuous display in Telephone Directory. Operation temperature of 20°C) Backup: 5 years if main batteries are replaced as soon as they become weak. 1 year if dead main batteries are left in the unit. • Note That the life of the battery that comes with the unit starts when the battery is loaded in the unit at the factory. The life you get from the battery may be shorter than normal because of the time the unit spends in transport, on the shelf, etc.
Auto power off:	Approximately 6 minutes after last key operation
Operating temperature:	0°C ~ 40°C (32°F ~ 104°F)
Dimensions:	Unfolded: 10.5H × 154W × 155.2mmD ($^3/_8$"H × 6"W × $6^1/_8$"D) Folded: 17.9H × 154W × 78mmD ($^3/_4$"H × 6"W × $3^1/_{16}$"D)
Weight:	152.5g (5.4 oz) including batteries

Current consumption:

Power switch	TYP. [μA]	MAX [μA]
OFF	8	29
ON	1,447	13,258
ON (Operating)	6,707	19,958

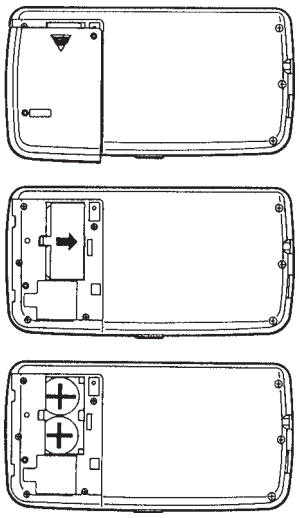
3. TO REPLACE THE BATTERY

A) To replace the main batteries

Before replacing the main batteries, note the following precautions.

- Do not remove the back-up battery from the SF Unit while main batteries are removed.
- Be sure to replace both batteries at the same time, and do not use an old battery with a new one.

1. Remove the screw that hold the battery compartment cover in place.
2. Remove the battery compartment cover by sliding it in the direction indicated by the arrow in the illustration.
3. Slide the main battery holder in the direction indicated by the arrow.
4. Remove both old batteries and replace with two new ones.
   - Use two new batteries. Wipe the surfaces of the batteries with a soft, dry cloth. Make sure that the positive (+) sides of the batteries are facing up (so you can view the positive sides as the batteries lie in the battery compartment).
5. Replace the battery holder.
6. Replace the battery compartment cover and fasten it in place using the screw.



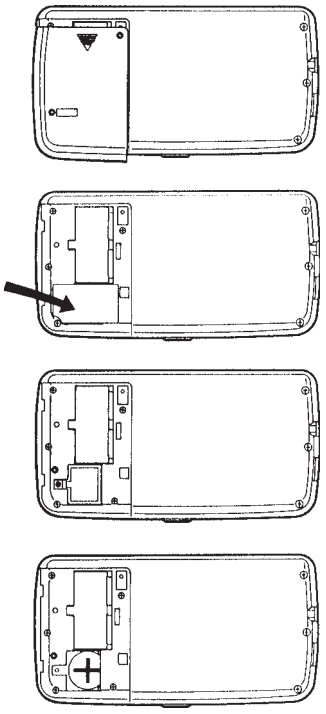
B) To replace the back-up battery

Before replacing the back-up battery, note the following precautions:

- Do not remove the main batteries from the SF Unit while back-up battery is removed.
- Be sure to replace the back-up battery at least once a year.

1. Remove the screw that hold the battery compartment cover in place.
2. Remove the battery compartment cover by sliding it in the direction indicated by the arrow in the illustration.
3. First , remove this sticker from the back-up battery holder.
4. After removing this sticker, take the screw off that secures the back-up battery holder in place, and then remove the battery holder.
5. Remove the old battery and replace it with a new one.
   - Wipe the surfaces of the battery with a soft, dry cloth.

   Make sure that the positive (+) side of the battery is facing up (so you can view the positive side as the battery lies in the battery compartment.)
6. Replace the back-up battery holder and fasten it in place using the screw, and replace the sticker over the battery holder.
7. Replace the battery compartment cover and fasten it in place using the screw.



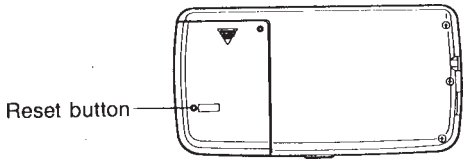
4. ERROR MESSAGE

Message	Meaning	Action
DATA ITEM NOT FOUND!	Text specified for search does not exist.	Correct or change specified text.
PASSWORD MISMATCH!	Wrong password entered.	Enter correct password.
MEMORY FULL!	No more room in memory for storage of data.	Delete unnecessary data items from memory.
DATA ERROR! CONSULT YOUR OWNER'S MANUAL UNDER "DATA ERROR"	Abnormal data caused by strong impact, static electricity, etc.	Consult the "DATA ERROR" section on page 2 of owner's manual.

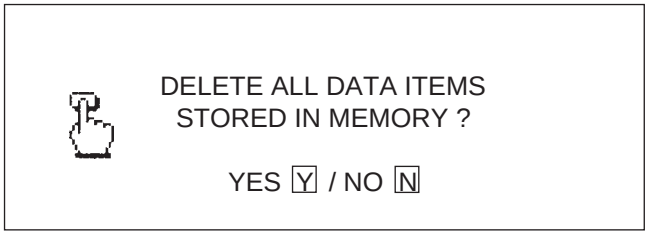
5. TO RESET THE DIGITAL DIARY

Before describing the RESET operation, a note of **WARNING — *The following procedure will erase all data stored in memory, including marked data items. Be sure to perform the RESET operation only if you wish to clear all data.***

To reset the SF Unit's memory



1. Switch on power and press the RESET button with a thin, pointed object.
   The following message appears on the display.



2. Press Y to reset the SF Unit and clear everything from its memory. To abort the procedure without clearing anything, press N .

Following the **RESET** operation, the Home Time Display appears. The initial settings of the SF Unit after reset are shown below.

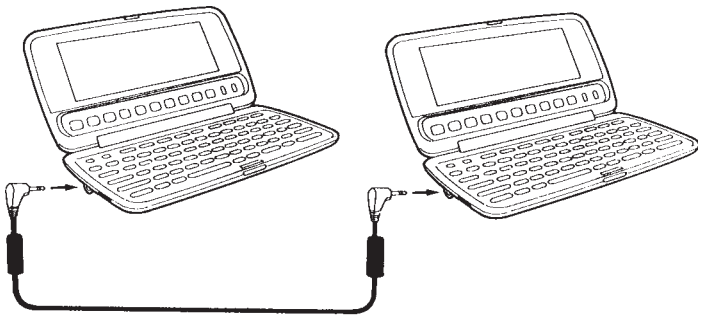
HOME TIME: Washington D.C.
JAN/1/1994 (SAT)
12:00 AM
12-hour format
WORLD TIME: New York
Daily Alarm: 12:00 PM
Sound: Schedule alarm ⟶ ON
Daily alarm ⟶ OFF
Key ⟶ ON
Character input: CAPS

6. TO SAVE THE DATA TO OTHER MACHINE

SF-8500 can transfer customers data to other SF-8500 with memory protection only when replacing the LCD or the outer case. How to transfer the data.

* Before connecting the cable (SB-60 or SB-62), be sure to reset the slave machine to clear all data.

1) Turn off the power switch and connect the two units using the cable (SB-60 or SB-62) as shown in the drawing.



SB-60/SB-62 cable

2) Turn on the power switch of each machine.

3) The slave machine must be set the date of Feb. 3rd, 1901 into the memory under the calculator mode.

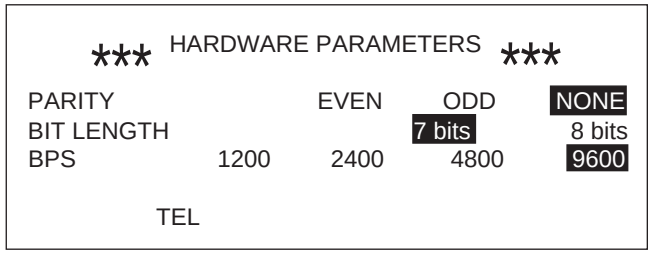
Operation: [ON] (CLEAR/AC) [CAL] [1] [9] [0] [1] [TIME DATE] [2] [TIME DATE] [3] [TIME DATE] [M+ R]

If you don't set the date, the "PASSWORD" isn't transferred to the slave machine.

4) Check the hardware parameters, and if the units have another condition, reset as follows.

To change the hardware parameters, press the ◁, ▷, △ and ▽ cursol keys.

To set the hardware parameters, press the set key.

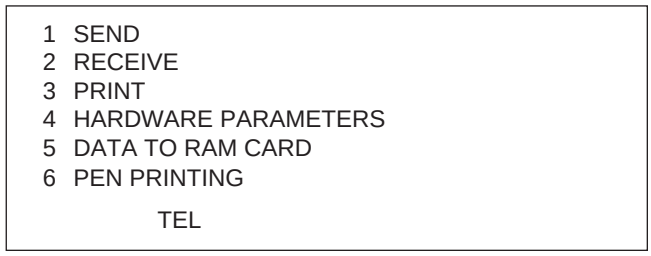


TEL FUNCTION 4 4

5) Set up the slave machine.

1 While in the Calendar Display, Telephone Directory, Business Card Library, Memo Mode, or Schedule Keeper, press the FUNCTION key followed by 4 to select " DATA COMMUNICATION", and the following menu appears.

TEL FUNCTION 4



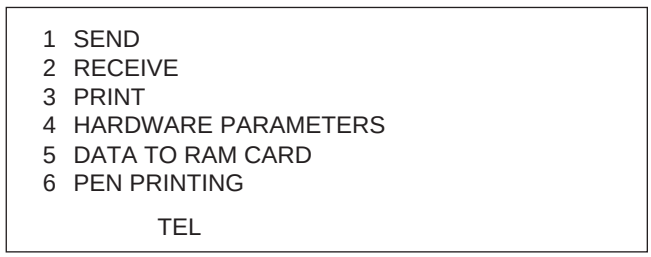
2 Press 2 to select "RECEIVE" and the following display appears to indicate that the slave machine is ready to receive data.

2

6) Set up the customer's machine.

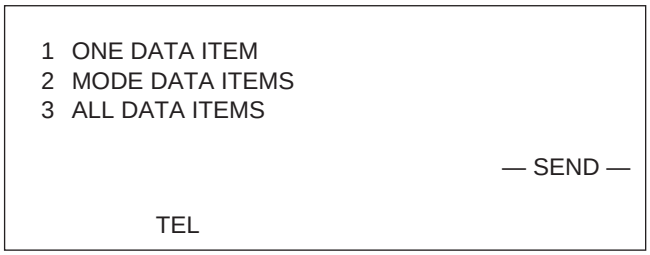
1 While the transmitting unit is in the Calendar Display, Telephone Directory, Business Card Library, Memo Mode, or Schedule Keeper, press the FUNCTION key followed by 4 to select "DATA COMMUNICATION", and the following menu appears.

TEL FUNCTION 4



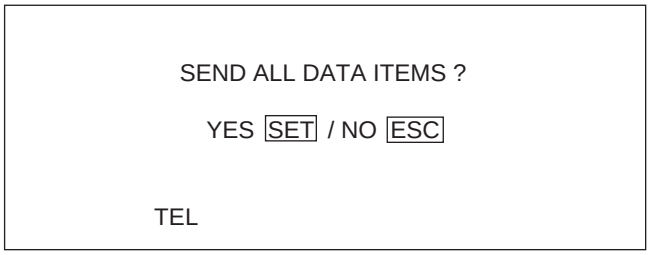
2 Press [1] to select "TRANSMIT" and the following menu appears.

[1]



3 Press [3] to select "ALL DATA ITEMS", and the following display appears to confirm whether you wish to proceed.

[3]



4 Press the [SET] key to proceed with the data transmission, or press [ESC] if you wish to cancel.

[SET]

Data are transmitted in the sequence of Telephone Directory data, Business Card Library data, Memo data, Schedule Keeper data and Calendar data.

* If the customer's machine uses full memory, it takes about one minute and ten seconds for this transferring.

* The following messages appear on the display of the receiving unit when a problem occurs during data communications. All data transferred up to display of the message is retained in memory, but data communication is terminated.
  If one of the following error messages appear, press the [TEL], [BUSINESS CARD], [MEMO], [SCHEDULE], [HOME TIME], [WORLD TIME], [CAL], [CALENDAR] key, to clear the error message. Then, take corrective action and try data communication again.

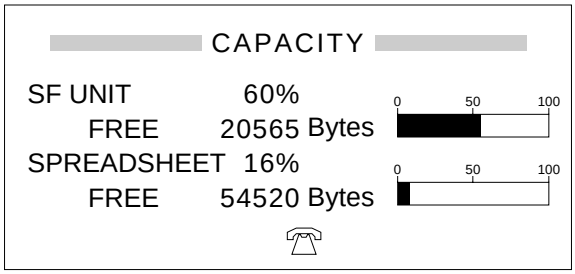
Message	Cause
STOPPED !	• [ESC] key pressed on transmitting or receiving unit. • Memory area of receiving unit full. • Battery power drops below a certain level.
TRANSMIT ERROR !	Cable connection broken or abnormal noise in cable.
MEMORY FULL !	Memory area of receiving unit full.

7. TO CHECK THE MEMORY CAPACITY

There are two types of Memory Capacity Display, as shown below:

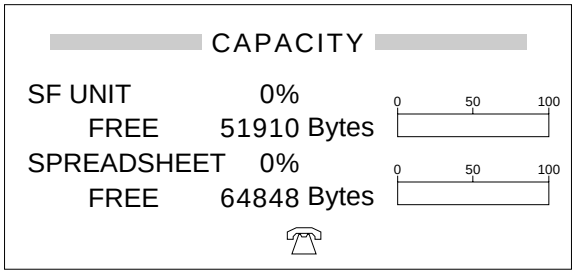
SF UNIT: Total memory used for storage of Telephone Directory, Business Card Library, Memo, Calendar, and Schedule Keeper data.

SPREADSHEET: Total memory used for storage of Spreadseet data.



Press the [SHIFT] key and then press the [CAPA] key to check the current memory capacity.

Following the memory reset operation, the display will appear as follows.

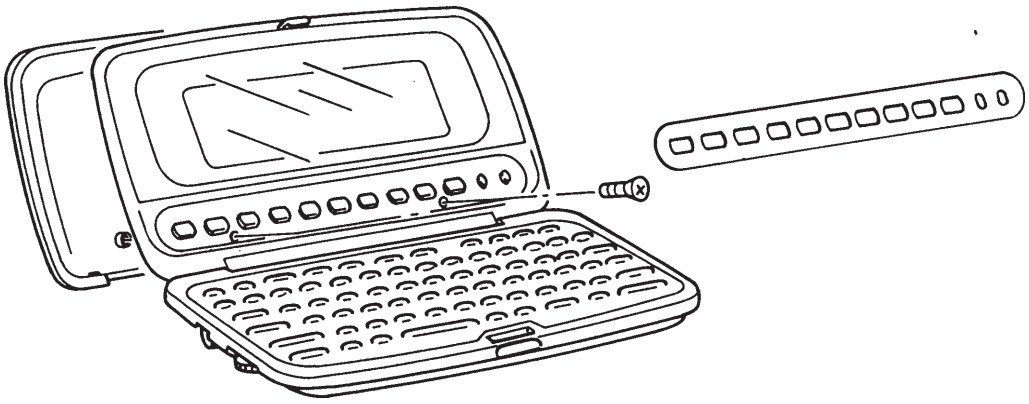


When the percentage of memory used reaches 100%, you will not be able to enter any more data into memory.

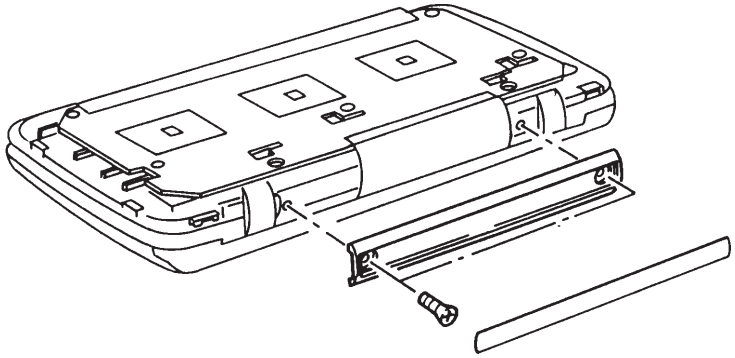
8. DISASSEMBLY (SF-8500)

1) To open display unit

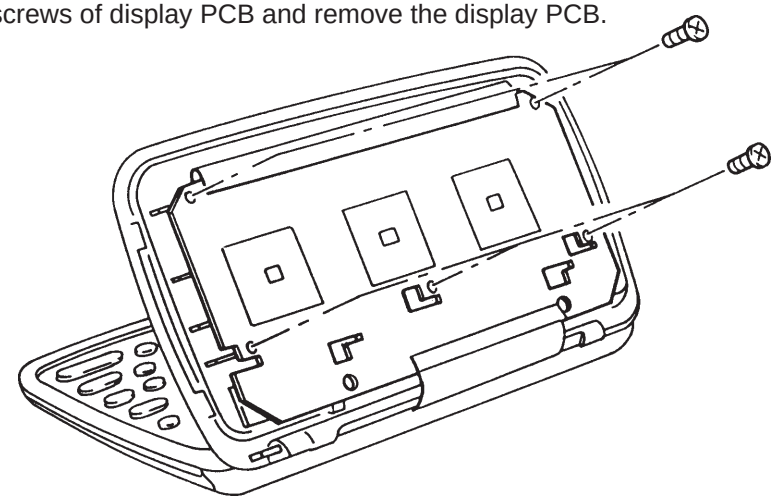
1. Remove the key switch sheet from the display frame with care using a sharp tweezers and remove 2 screws, then remove the display back cover.



2. Remove the blind plate of hinge and then release the 2 screws of hinge cover.

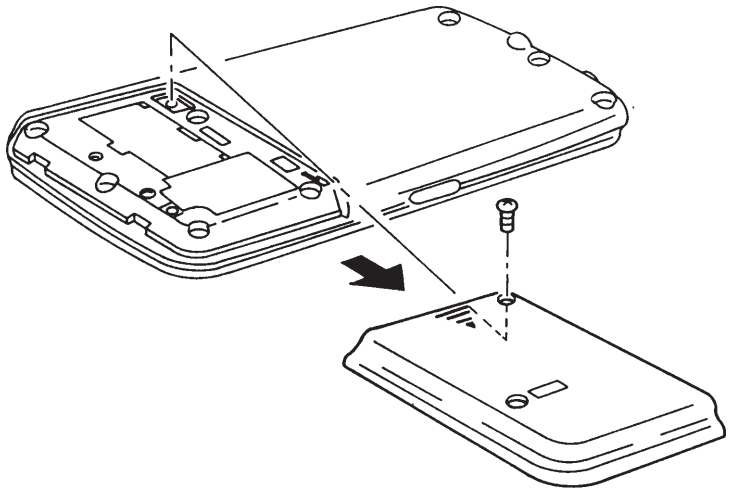


3. Release the 5 screws of display PCB and remove the display PCB.



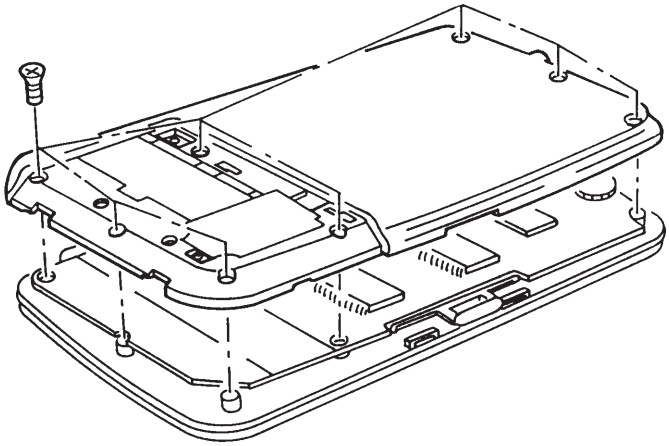
2) To open battery cover and back cover

1. Release the one screw of battery cover and remove the battery cover.

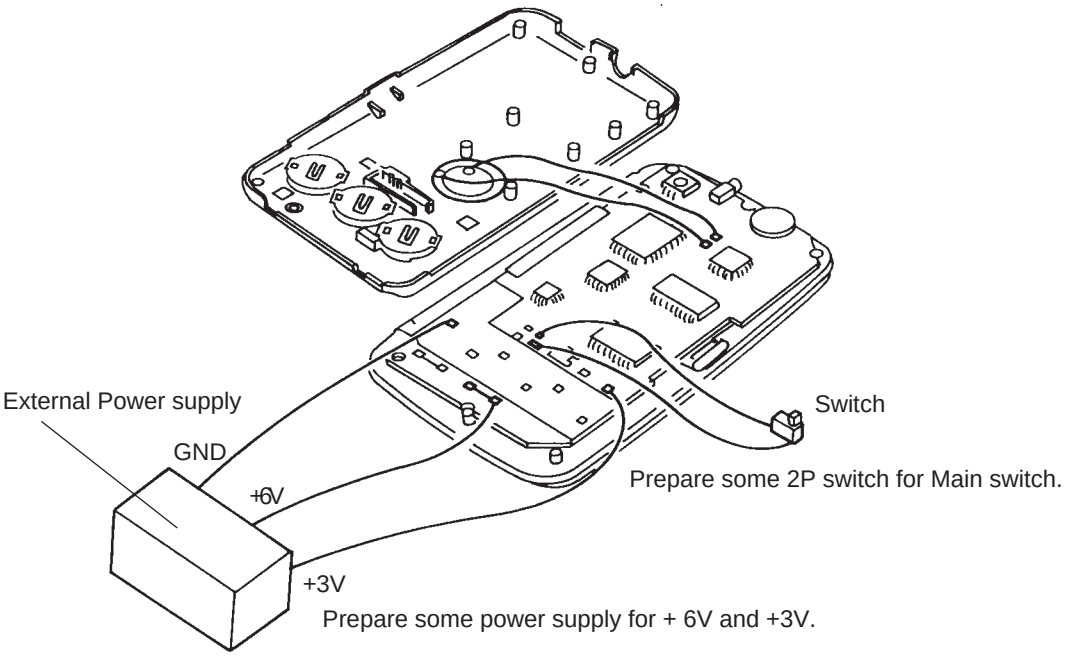


2. Remove the batteries. (Refer section 3 in this manual.)

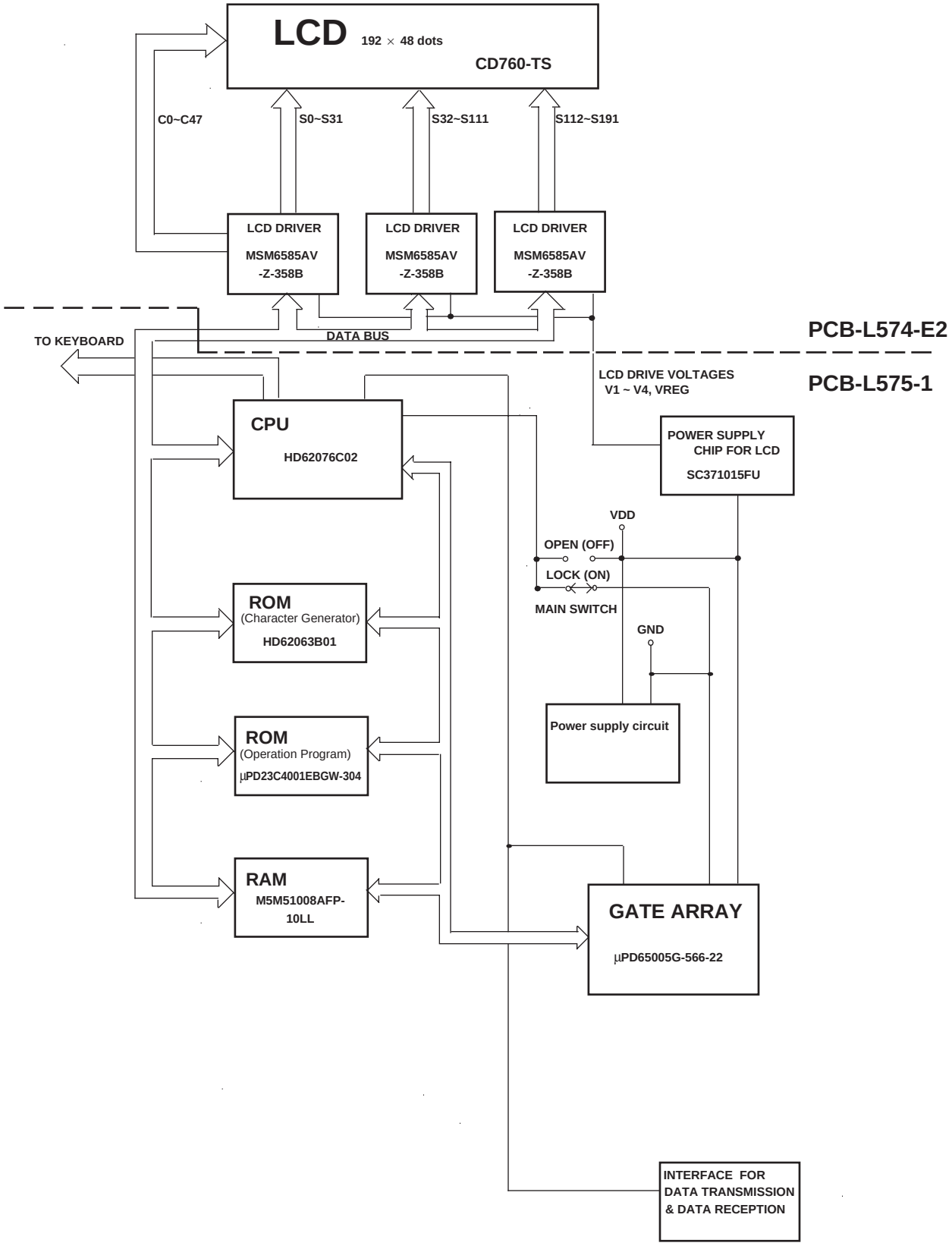
3. Release the 8 screws of the back cover. Then, remove the back cover.



4. To check the circuit by oscilloscope, apply the power to main PCB as follow:



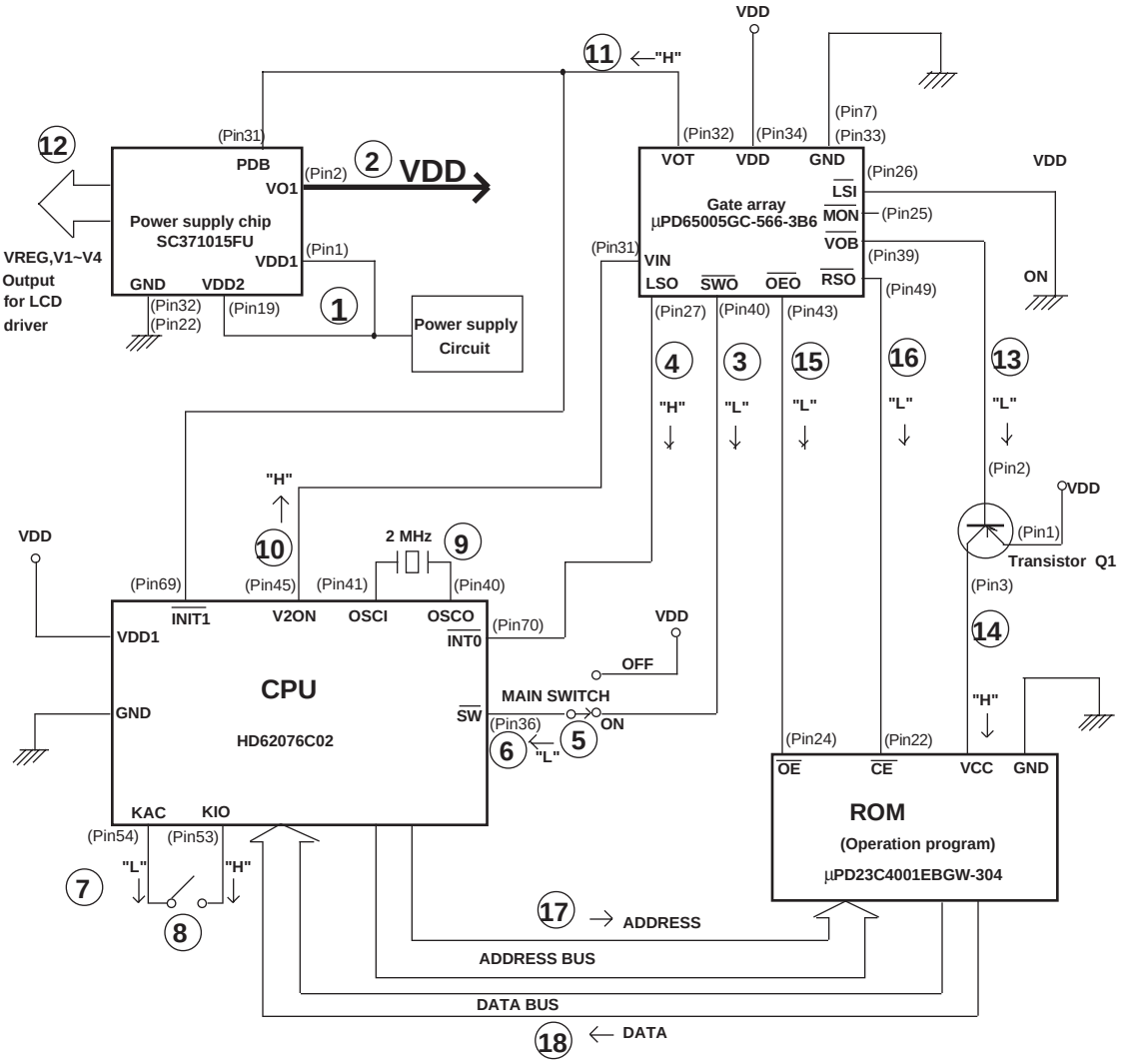
9. BLOCK DIAGRAM



10. CIRCUIT EXPLANATIONS

10-1. System chart

Generally, SF-8500 is working with the following steps.



1. Supply 5V to VDD1 and VDD2.
2. Output VDD (4.5V).
3. Output "L" from $\overline{\text{SWO}}$ terminal.
4. Output "H" from LSO terminal.
5. Main switch ON.
6. Input "L" to $\overline{\text{SW}}$ terminal.
7. Output "L" from KAC terminal.
8. Push power on button switch.
9. CPU oscillation is generated.
10. Output "H" from V2ON terminal.
11. Output "H" from VOT terminal.
12. Output all LCD drive voltages.
13. Output "L" from $\overline{\text{VOB}}$ terminal.
14. Apply VDD to ROM.
15. Gate array sends ROM output enable signal from $\overline{\text{OE}}$ terminal.
16. Gate array sends ROM Chip enable enable signal from $\overline{\text{CE}}$ terminal.
17. CPU sends address to ROM.
18. CPU receives data from ROM.

10-2. Power supply circuit

1) Power supply circuit for CPU, GATE ARRAY, CG ROM and RAMs.

When the memory back-up battery or main batteries are set, the voltage supplies at the terminal VDD1 (Pin No.1) of SC371015FU (LSI2) through the diode MA743 (D1).
When LSI2 receives a voltage, the regulated voltage VDD (4.3V~4.7V) will be applied to the VDD lines from the terminal VO1 (Pin No.2).
HD62076C02 (LSI1), μPD65005GC-566 (LSI3), HD62063B01 (LSI4), and M5M51008AFP-10LL (LSI5) are connected the VDD lines.

2) Power supply circuit for ROMs

When the GATE ARRAY (LSI3) controls the terminal VOB (Pin No.39) with "L" level, the transistor 2SA1411 (Q1) will be turned ON, then the voltage of the VDD lines will be applied the VCC lines.
The voltage of the ROM (LSI6) is supplied from the VCC lines.

3) Main switch

The CPU (LSI1) detects the informations of the Main switch by the terminal SW (Pin No.36) from the SWO signal of the GATE ARRAY (LSI3).

4) How to turn the display ON.

When pressing "ON" key under the ON side of the Main switch , the CPU (LSI1) generates the signal to turn the display ON at the terminal V2ON (Pin No.45).
This signal goes to the terminal VIN (Pin No.31) of the GATE ARRAY (LSI3), then the GATE ARRAY (LSI3) generates "H" level at the terminal VOT (Pin No.32). When the power supply chip (LSI2) receives "H" level at the terminal PDB (Pin No.31) from VOT, the LSI2 generates the outputs VSS (Pin No.8) and V1~V4 (Pin No.9~12) for LCD drivers.

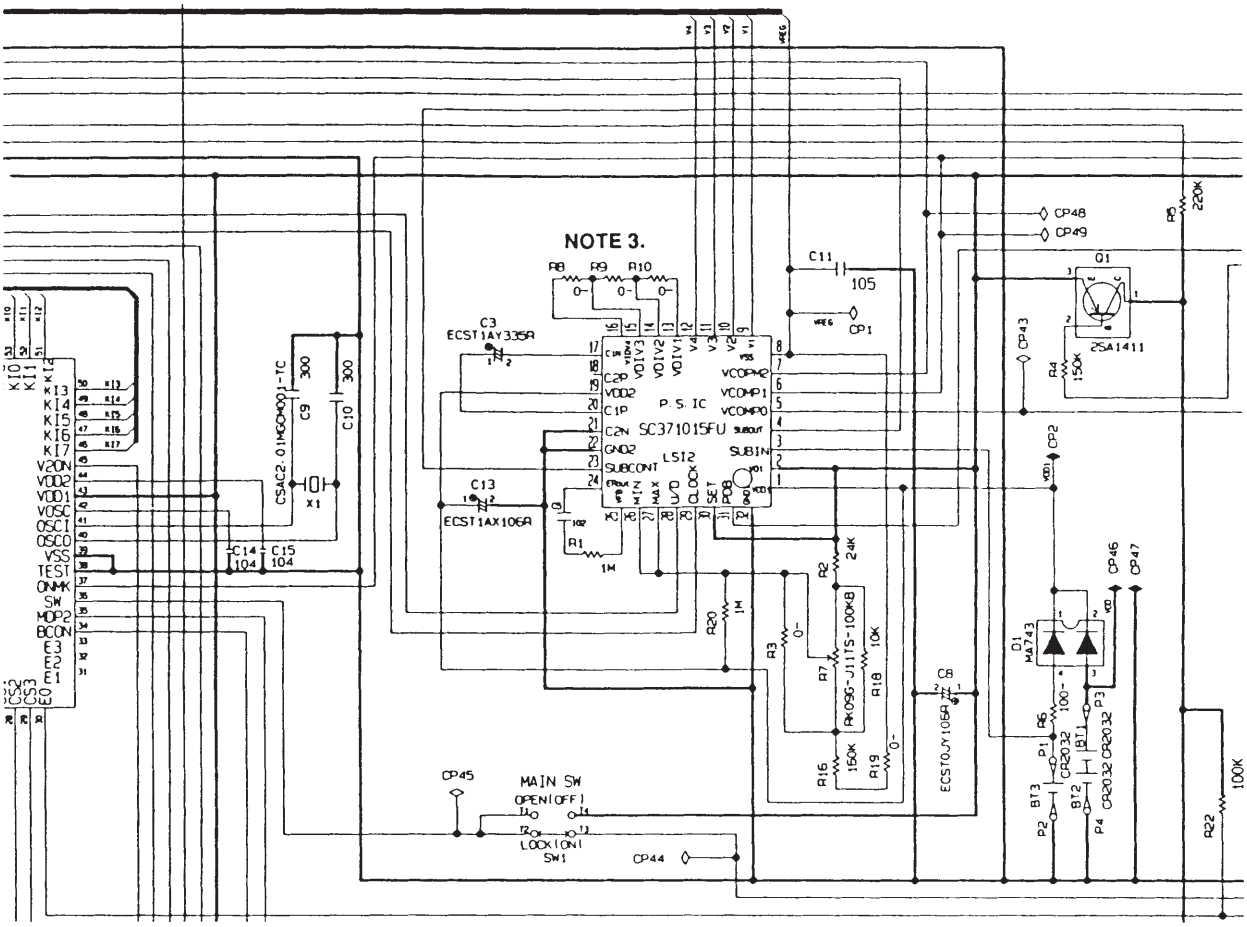
5) How to detect the voltage for the main batteries.

There are three detectors of the main batteries in the circuits.
When the voltage of the VDD lines becomes +4.58V±0.155V, the terminal VCOMP2 (Pin No.7) of the power supply chip (LSI2) becomes "L" level, then this signal goes t the terminal P7 (Pin No.79) of the CPU (LSI1) and the terminal BLI (Pin No.29) of the GATE ARRAY (LSI3).
The CPU detects the low battery condition, and the display shows "MAIN POWER SUPPLY GETTING WEAK".
When the voltage of the VDD lines becomes +4.38V ±0.155V, the terminal VCOMP1 (Pin No.6) of the power supply chip (LSI2) bocomes "L" level, and the terminal BLI (Pin No.29) of the GATE ARRAY (LSI3) receives this shignal, then the display turns OFF.

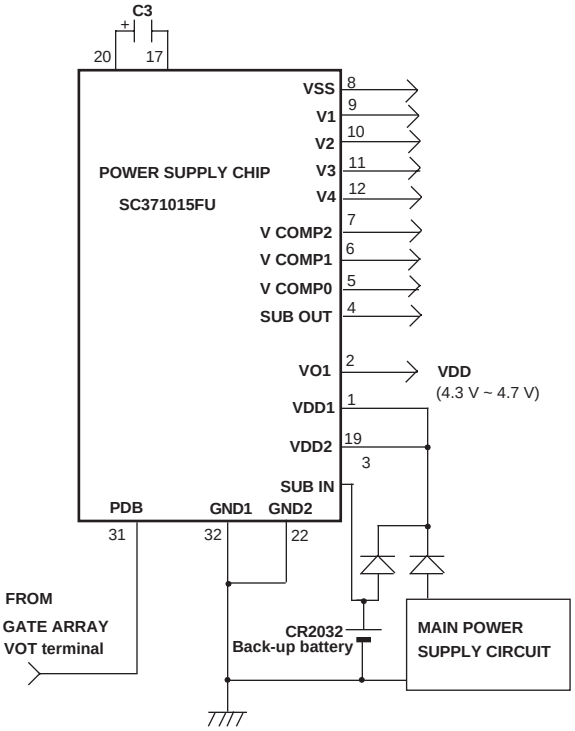
When the voltage from the main batteries becomes +3.7V ±0.1V, the terminal VCOMP0 (Pin No.5) of the power supply chip (LSI2) becomes "L" level, then this signal goes to the terminal PDN (Pin No.28) of the GATE ARRAY (LSI3). After this, the terminal VOT (Pin No.32) of GATE ARRAY (LSI3) become "L" level, and the terminal PDB (Pin No. 31) of the power supply chip (LSI2) receives this signal.
In this condition, the voltages for LCD will be cut off compulsorily.
When the voltage from the memory back-up battery becomes +2.5V±0.065V, the terminal SUBOUT (Pin No.4) of the power supply chip (LCI2) becomes "L" level, and the terminal P6 (Pin No.78) of the CPU (LSI1) detects the low battery condition. The display shows "MEMORY BACKUP BATTERY GETTING WEAK".

6) Others

The voltages of the circuit are applied from the main batteries or the memory back-up battery by the diode MA743 (D3). The voltage of memory back-up is also provided with the main batteries.



7) Power supply chip SC371015FU



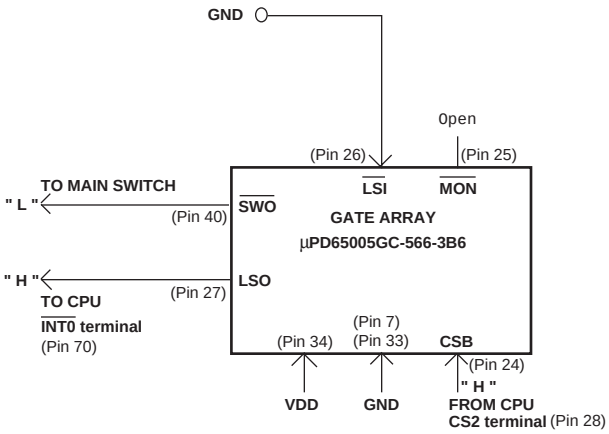
The IC SC371015FU is power supply chip for SF-8500. When IC SC371015FU receives a Voltage 5V from main power supply circuit at the terminal VDD1(Pin No.2), the regulated voltage VDD (4.3~4.7V) will be applied to the VDD lines. The outputs VSS (VREG) and V1~V4 are the LCD drive voltages. When the terminal PDB becomes "H", those voltages are generated by IC SC371015FU and capacitors C3 and applied to LCD driver IC MSM6385AV-Z-358B.
The voltages for LCD driving are shown below:

LCD DRIVE VOLTAGE	Value (Approx.) [V]	
	Contrust : Min.	Contrust : Max.
VSS(VREG)	-3.07	-5.27
V1	+3.50	+3.23
V2	+2.57	+2.02
V3	-1.16	-2.80
V4	-2.11	-4.04

The V comp0 ~ V comp2 and Sub out outputs are the battery voltage detection outputs. According to VDD1 and VDD2 voltages, those outputs will change the status as follows:

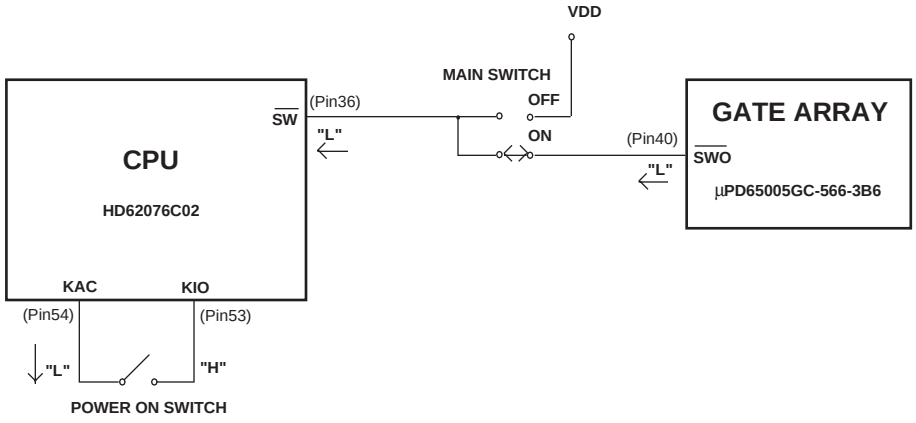
OUTPUTS	STATUS "H"	STATUS "L"	NOTE
V COMP 0	When the VDD1,2 voltages are more than 3.7±0.1V.	When the VDD1,2 voltages are less than 3.7±0.1V.	Switch off the LCD driving voltages
V COMP 1	When the VDD1,2 voltages are more than 4.38±0.155V.	When the VDD1,2 voltages are less than 4.38±0.155V.	Main battery check
V COMP 2	When the VDD1,2 voltages are more than 4.58±0.165V.	When the VDD1,2 voltages are less than 4.58±0.165V.	Main battery check
SUB OUT	When the SUB IN voltage is more than 2.5±0.065V.	When the SUB IN voltage is less than 2.5±0.065V.	Back-up battery check

8) Gate array



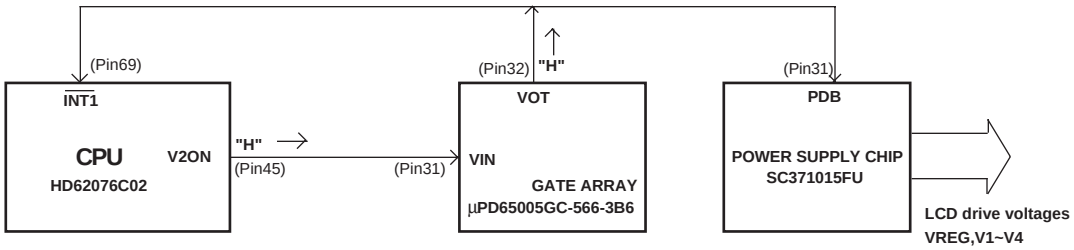
When VDD is applied from power supply IC SC371015FU to gate array µPD65005GC-556-3B6, gate array will send "L" signal to active the main switch signal from terminal $\overline{SWO}$.
Also, gate array will send "H" signal to release the $\overline{INT0}$ terminal of CPU from LSO terminal.
The terminal CSB is for the chip select of gate array. This signal is sent from CPU terminal CS2. And when the VDD is applied to CPU, CPU will send "H" signal to CSB terminal.

9) Main switch and power on switch



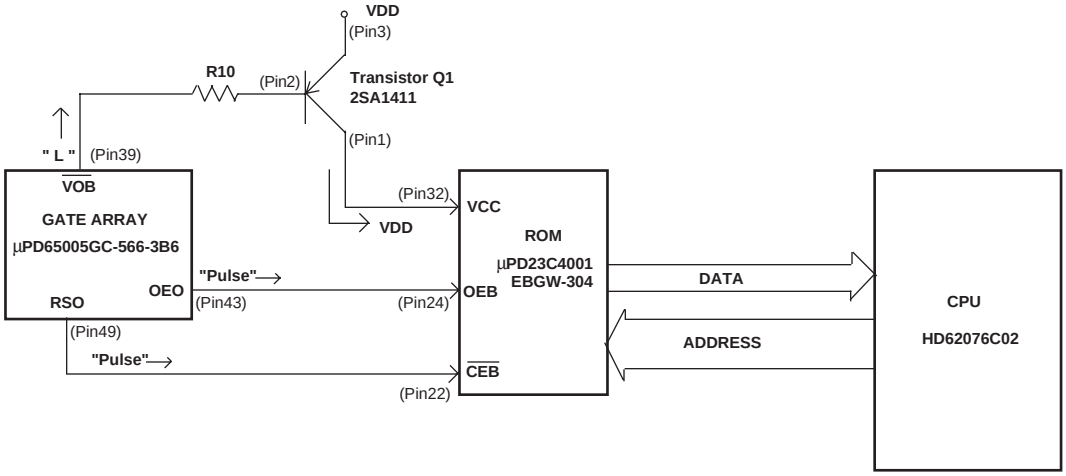
When the main switch is set to on position, $\overline{SW}$ terminal of CPU becomes "L", then CPU will send "L" signal to KAC terminal to enable the system power on. The KI0 terminal is "H" when VDD is applied to CPU. Therefore, when pressing the power on switch, CPU will generate a clock pulse (2 MHz) for start up the system.

10) Power supply for LCD



When the system is start up, CPU will send "H" signal to VIN terminal of gate array from V2ON terminal. Then, gate array will send "H" signal from VOT terminal to release interruption signal $\overline{\text{INT1}}$ of CPU and also, it will be sent to PDB terminal of power supply chip to generate LCD drive voltages.

11) ROM driving transistor



After gate array send VOT signal, gate array send "L" signal from $\overline{\text{VOB}}$ terminal to base terminal of transistor Q1. Then, the VDD is applied to ROM (operation program), CPU can read a ROM program data.

10-3. CPU pin description (HD62076C02)

Pin No.	Name	In/Out	Status of OFF	Status of ON	Description
1~14,16,17	A0~A15	Out	L	Pulse	Address Bus line
15,39, 100	VSS	In	GND	GND	GND terminal
24	WE	Out	H	Pulse	Write signal
25	OE	Out	H	Pulse	Read signal
26	FE	Out	H	Pulse	Not used
27	CS1	Out	H	H	Not used
28	CS2	Out	H	H	Chip select signal for gate array
29	CS3	Out	H	Pulse	Chip select signal for ROM (Charactor generator)
30	E0	Out	L	Pulse	Chip enable signal for ROM (Operation program)
31	E1	Out	L	H	Chip enable signal (Not used)
32	E2	Out	L	H	Chip enable signal (Not used)
33	E3	Out	L	H	Chip enable signal (Not used)
34	BCON	Out	H	H	BCN signal to gate array
35	MDP2	Out	H	L	MDP signal to gate array
36	SW	In	L	L	Switch signal (When switches are at ON position)
37	ONMK	In	H	H	Battery detection V comp1 input
38	TEST	In	L	L	TEST terminal (connect to GND)
40,41	OSC O/I	In	L	Pulse	Clock input
42	VOSC	In	L	H	Power input for Clock
43, 91	VDD1	In	H	H	VDD input terminal
44	VDD2	In	H	H	VDD input terminal
45	V2ON	Out	L	H	Power on output signal
46~53	KI7~KI0	In	H	H	Key input signal (K17…Not used)
54	KAC	Out	L	Pulse	Power on switch signal output
55~65,67	KC0~KC11	Out	H	Pulse	Key common signal output
66	GND	In	L	L	GND terminal
68	INT2	In	H	H	Interrupt signal from ROM (Charactor generator)
69	INT1	In	L	H	Interrupt signal for transmission
70	INT0	In	H	H	Interrupt signal for transmission
71	BRK	In	H	H	VDD input terminal
72	P0	Out	H	H	Transmission data output
73	P1	In	L	H	Reception data input
74	P2	In	H	H	Card lock switch input
75	P3	In	L	H	IC card detection signal input
76	P4	Out	H	Pulse	KC 12 key common signal output
77	P5	Out	H	Pulse	KC 13 key common signal output
78	P6	In	H	H	Memory back-up battery detection input
79	P7	In	H	H	Battery detection V comp2 input
80	H1	Out	H	H	Display contrast control signal output (Up/Down)
81	WENL	In	L	L	GND terminal
82	H2	Out	H	H	Not used
83	L1	Out	L	H	Chip enable signal for gate array
84	L2	Out	L	L	Dispray contrast control clock signal
85	DT	Out	H	Pulse	Not used
86	PRO	Out	L	H	LCD driver mode selection signal
87	FR	Out	L	Pulse	LCD driver synchronous signal
88	LP	Out	H	Pulse	LCD driver latch pulse signal
89	GC	Out	H	Pulse	GC signal output
90	DE	Out	H	Pulse	LCD driver data latch clock signal
92~99	IO7~IO0	In/Out	L	Pulse	Data bus line
18~23	RA14~19	Out	L	Pulse	Address line (Used exept RA 14)

10-4. Gate array pin descriptions (μPD65005GC-566-3B6)

Pin No.	Name	In/Out	Status of OFF	Status of ON	Description
1~6, 8, 9	OI7~OI0	In/Out	L	L	Not used
7, 33	GND	In	L	L	GND terminal
10	B15	In	L	Pulse	Address input
11~13	A15,A01,A00	In	L	Pulse	Address input
14	N.C.	-	-	-	Not used
15	DT	In	H	Pulse	GC signal input
16~23	IO0~IO7	In/Out	L	Pulse	Data bus line
24	CSB	In	H	Pulse	Chip select signal from CPU
25	MON	Out	L	L	Not used
26	LSI	In	L	L	Connected to GND
27	LSO	Out	H	H	Always "H"
28	PDN	In	H	H	Power down detection input
29	BLI	In	H	H	Battery detection V comp1 input
30	DEB	Out	H	Pulse	Chip selection signal for ROM (Charactor generator)
31	VIN	In	L	H	Power on signal input
32	VOT	Out	L	H	Power on signal output
34	VDD	In	H	H	VDD terminal
35	OEI	In	H	Pulse	Read signal input
36	WEI	In	H	Pulse	Write signal input
37	BBC	Out	L	Pulse	Memory back-up battery scanning signal
38	CDE	In	L	H	IC card detection signal input
39	VOB	Out	H	L	ROM power switching signal (Operation program)
40	SWO	Out	L	L	Main switch control signal
41	BCN	In	H	H	BCON signal from CPU
42	MDP	In	H	L	MDP2 signal from CPU
43	OEO	Out	L	Pulse	Read signal for ROM
44	WEO	Out	L	Pulse	Not used
45, 51	A19, A16	In	L	Pulse	Address input
46, 47	R15, R16	Out	L	Pulse	Address output
48	EOB	In	H	Pulse	Chip enable signal from CPU
49	RS0	Out	H	Pulse	Chip enable signal for ROM (μPD27C4001EBGW-304)
50	CS3	In	H	Pulse	Chip select signal from CPU
52	RS3	Out	H	Pulse	Chip enable signal for ROM (Character generator)

10-5. Power supply chip IC pin descriptions (SC371015FU)

Pin No.	Name	In/Out	Status of OFF	Status of ON	Description
32, 22	GND1, 2	In	L	L	GND terminal
1, 19	VDD1, 2	In	H	H	Main battery positive terminal (+5V)
2	Vo1	Out	H	H	VDD output terminal (4.5V)
31	PDB	In	L	H	Power on switch signal from gate array

Pin No.	Name	In/Out	Status of OFF	Status of ON	Description
3	SUB IN	In	+3V	+3V	Back-up battery detection input
4	SUB OUT	Out	H	H	Back-up battery detection output (less than 2.5V…"L")
5	V COMP0	Out	H	H	Battery detection signal (less than 3.7V…"L")
6	V COMP1	Out	H	H	Battery detection signal (less than 4.4V…"L")
7	V COMP2	Out	H	H	Battery detection signal (less than 4.7V…"L")
8	VSS	Out	H	-7V	LCD drive power VREG
9	V1	Out	L	3V	LCD drive power V1
10	V2	Out	L	2V	LCD drive power V2
11	V3	Out	H	-5V	LCD drive power V3
12	V4	Out	H	-6V	LCD drive power V4
13~16	VDIV1~4	**	H	Wave	Voltage dividing terminal for LCD drive power
17	C1N	**	GND	Wave	Negative terminal for doubler capacitor C3
18	C2P	**	3V	Wave	Not used
20	C1P	**	3V	Wave	Positive terminal for doubler capacitor C3
21	C2N	**	GND	Wave	GND
23	SUB CONT	In	L	L	Back-up battery detection clock input
24	EROUT	Out	H	Wave	LCD drive basic voltage output
25	VFB	**	H	Wave	LCD drive basic voltage input
26	MIN	In	5V	5V	LCD drive MIN voltage setting terminal
27	MAX	In	%v	5V	LCD drive MAX voltage setting terminal
28	UPDOWN	In	H	H	LCD contrast control signal input (Up/Down)
29	CLOCK	In	L	L	LCD contrast clock signal input
30	SET	In	H	H	Switch signal for contrast ("L"…software, "H"…hardware)

10-6. Character generator ROM pin descriptions (HD62063B01)

Pin No.	Name	In/Out	Status of OFF	Status of ON	Description
1, 7~12, 23	NC	**	**	**	Not used
2	BLD	In	L	L	Not used (Battery voltage detection terminal)
3	VOSC	In	3V	3V	Connected capacitor
4, 20	GND	In	L	L	GND terminal
5, 6	OSI/OSO	In	Pulse	Pulse	Exterminal clock terminal (32.768 KHz)
13	TNL	Out	**	**	Not used
14, 19	IN1+, IN2+	In	H	H	Connected to VDD
15, 32	VSS1, VSS2	In	L	L	GND terminal
16, 21	IN1-, IN2-	In	H	H	Connected to VDD
17, 22	OUT1, OUT2	Out	**	**	Not used
18	TNH	Out	**	**	Not used
24	IN	In	L	Pulse	Power on key input terminal
25	OUT	Out	H	Pulse	K10 terminal for power on
26` 27	BZ1, 2	Out	L	L	Buzzer signal
28	INT	Out	H	H	Interrupt signal for alarm clock (alarm time…"L")
29, 30	CEH, CEL	Out	H	Pulse	RAM chip select signal
31	CED	In	H	Pulse	Chip enable signal from CPU
33	EN	In	L	H	Enable signal (Buzzer off…"L")
34~37	IO3~IO0	In/Out	L	Pulse	Data bus line (IO0~IO3)
38~42	A0~A3, A15	In	L	Pulse	Address bus line (A0~A3, A15)
43	WEB	In	H	Pulse	Write signal
44	CSB	In	H	Pulse	Chip select signal

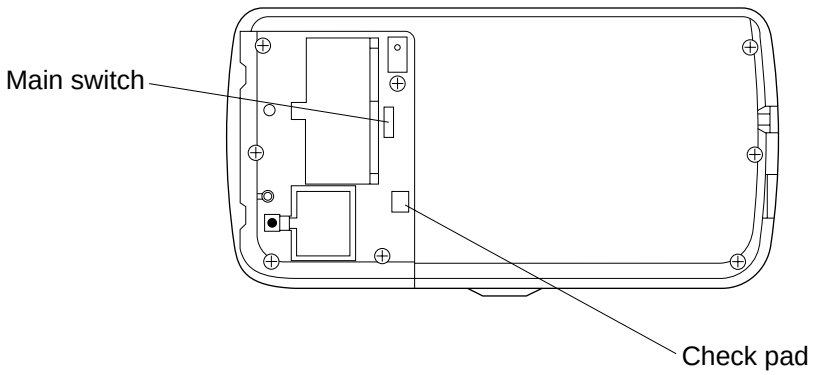
10-7. Operation program ROM pin discriptions (μPD23C4001EBGW-304)

Pin No.	Name	In/Out	Status of OFF	Status of ON	Description
2~12,23, 25~31	A0~A18	In	L	Pulse	Address bus line (A0~A14, RA15~RA18)
13~15, 17~21	O0~O7	Out	L	Pulse	Data bus line (IO0~IO7)
16	GND	In	L	L	GND terminal
22	CEB	In	H	Pulse	Chip enable signal from Gate array
24	OEB	In	L	Pulse	Output enable signal from Gate array
1, 32	N.C., VCC	In	L	H	VDD terminal

10-8. RAM pin discriptions (M5M51008AFP-10LL)

Pin No.	Name	In/Out	Status of OFF	Status of ON	Description
2~12,23, 25~28, 31	A0~A16	In	L	Pulse	Address bus line (A0~A14, RA15, RA16)
13~15, 17~21	O0~O7	Out	L	Pulse	Data bus line (IO0~IO7)
16	GND	In	L	L	GND terminal
22	CS1	In	H	Pulse	Chip enable signal from Gate array
24	OEB	In	L	Pulse	Output enable signal from Gate array
1, 32	N.C., VCC	In	L	H	VDD terminal
29	WEB	In	H	Pulse	Write enable signal from CPU

11. DIAGNOSTIC OPERATION



SELECT MENU	1 DISPLAY
	2 MEMORY
	3 KEY
	4 BUZZER
	5 I/F

1. Diagnostic mode

The diagnostic mode appears when main switch is turned on while there is a short in the checkpad. After this operation, the machine will beep and display "SELF-TEST".

The menu appears after press SET key. Tests are conducted by selecting the mode from the list on screen. The each test can be selected by the following function keys.

SPREADSHEET key	: Test the LCD display
TEL key	: Test the IC memory chip and the RTC
BUSINEESS CARD key	: Test all keys
MEMO key	: Buzzer test
SCHEDULE key	: SB-60/SB-62cable interface

DISPLAY	1 WHITE
	2 BLACK
	3 CHECKER
	4 REVERSE
	5 FRAME

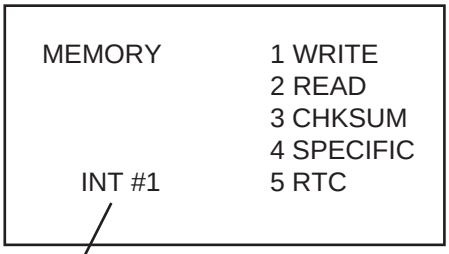
2. Display check

DISP CHNG key : Return to menu display

SPREADSHEET key	: Lights on dot at corners
TEL key	: Lights on in all dots (black screen)
BUSINEESS CARD key	: Checker display
MEMO key	: Reverse checker display
SCHEDULE key	: Lights on dot along the screen edge (frame)

3. ROM/RAM check

DISP CHNG key :Return to menu



INT---Internal RAM
EXT--External RAM(RAM card)
#1---Test data pattern(00,01,02...)
#2---Test data pattern(FF,FE,FD....)

SPREADSHEET key	: Write the set pattern to the selected RAM area
TEL key	: Compare the pattern displayed after # with the write data of RAM and displays the results.
BUSINESS CARD key	: Dump contents of memory. (direction depens on setting of internal/ extarnal switch)
MEMO key	: Call up checksum and XOR values for connected ROM/RAM data.
SCHEDULE key	: Bring up clock display. The present time, data and daily alarm can be set.

NOTE 1. To change the RAM internal or extenal, press HOME/WORLD key. As SF-8500 has no RAM card interface, Test only Internal RAM area.

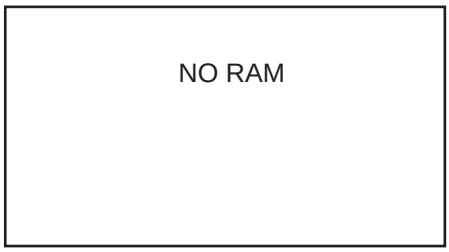
NOTE 2. To change the test data pattern,
press CALENDAR key for data pattern 1 (00,01,02,03,.....FF,00,01,02,03,.....).
press HOME/WORLD key for data pattern 2 (FF,FE,FD,.....00,FF,FE,FD,.....).

1) RAM write

The machine will beep after 3 seconds.
The menu is unchanged.

It means RAM write is succeeded.

When there is no RAM to write a data, the following message will be displayed.

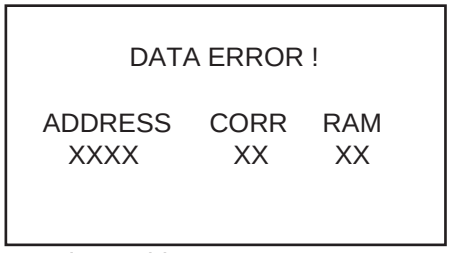


To release this message, press DISP CHNG key.

2) RAM read

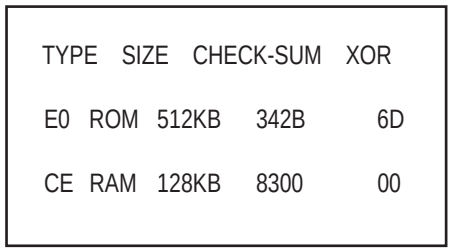
Normal end display is;

Error end display is;



To release this message, press DISP CHNG key.

3) CHECK SUM



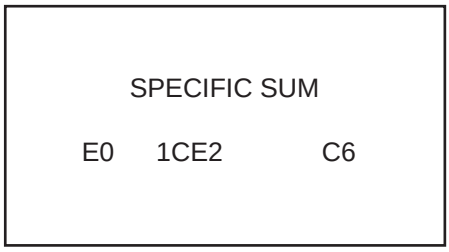
When memory dump is operated by pressing BUSINESS CARD button, a display will appear as shown at left. The first two lines, begining from the top left, signify the following address values in reference to the one megabyte "E0" area:
00001,00002,00004,....,00080,00100,00200
00400,00800,01000,....,20000,40000,80000
The lower two lines refer to the data in the "E1" area.

Type : ROM and RAM are shown. However, if the ROM is not in standard Casio format, a format error will be displayed.
Size : Memory capacity (total)
Checksum:
XOR : Logic operation for all data.

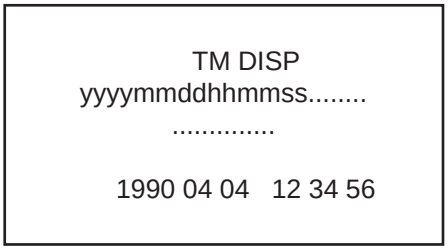
The ON key is the only key that remains functional when an error has occurred or check-sum is being displayed.

Note: The Internal/External switch is activated pressing CAL button. SF8500 has no external RAM area.

4) SPECIFIC (ROM check)

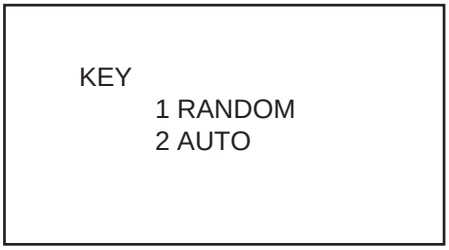


5) RTC



Input can be made in the second and third lines using the numeric keys. Entry of 12 or more digits sets the time and date. Entry of 4 or 6 digits sets the daily alarm. The ON key clears current entries.

4. Key check

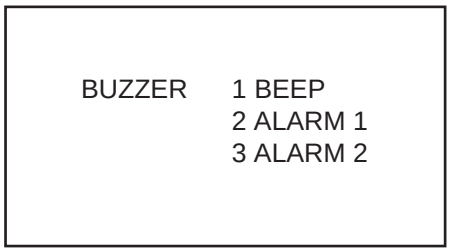


SPREADSHEET Key :
The 'key code' will be displayed.
The 'key code' is numbered incrementally from left to right with the DISPLAY CHANGE key as "00", and TEL key as "02" etc. Accordingly, the SET keys is "81". To release this test, press SEARCH key.

TEL key :
Limits the mode mentioned above so that the keys must be pressed in order according to the key code. If an error is made a buzzer sounds for about 1 second. (A correct entry results in a beep tone)

In either mode a press of the SEARCH key will return the screen to the menu mode.

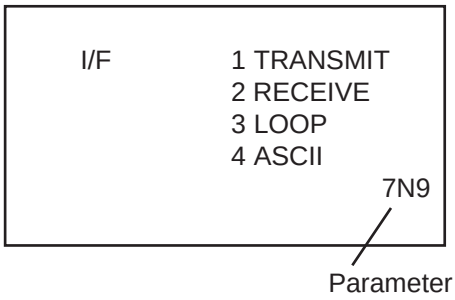
5. Buzzer check



SPREADSHEET key : Key input sound every 1 second
TEL key : Sound alarm 1
BUSINESS CARD key : Sound alarm 2

Sound can be stopped by pressing the any key.
While an alarm is sounding the screen display is as shown at left. If an irregularity is found in voltage of battery while the alarm is sounding, the alarm will stop. After 256 seconds, the alarm will stop automatically.

6. SB-60/SB-62 cable interface check



The SPREADSHEET to MEMO keys are used to select mode; the CALENDAR, SCHEDULE and HOME/WORLD key are used to set the transmission paraments. The three charactors that appear on the right side at display represent the parameter. In the case of the exampledisplay, it indicates 7 BIT, NON PARITY, 9600 BPS. The operation continues until stopped by pressing the ESC key and then pressing the ON key for all modes.

DISP CHNG key : Return to menu mode
SPREADSHEET key : Transmission mode. The data of transmission is "H" and it is sent out by the data of & H34 and & H38 by the Xon/Xoff control.
TEL key : Reception mode. Make sure to set the parameter to match that of the transitting side. The data received appears on the display.
BUSINESS CARD key : Loop back test. Short the Tx and Rx terminals for this test. Transmit and check from &H20 to &H7E. When complete, the message 'CHECK COMPLETE' is displayed.
MEMO key : Output the following ASCII code by Xon/Xoff control.

```
!"#*+,-/0123456789:
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
```

A line end code is added with each line.

SCHEDULE key : Switch the data length 7 bit(7) or 8 bit(8)

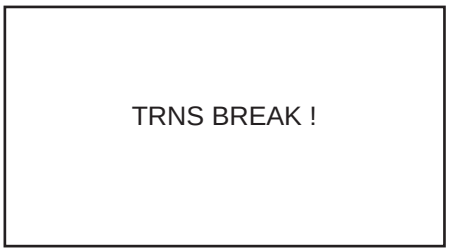
CALENDAR key : Switch the parity bit : NON(N)—EVEN(E) —NON(N) —ODD(O)

HOME/WORLD key : Switch the transmission speed : 9600(9)—4800(4)—2400(2)—1200(1)

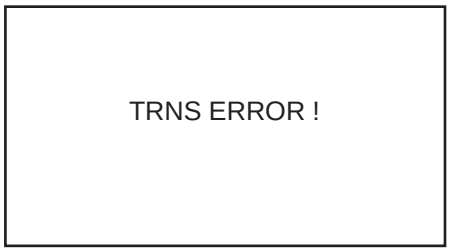
To communicate two machines, please set the transmission machine before setting the receiving unit. To release communication, press ESC button. In this case, the break code is sent to receive units. Therefore, both machines display "TRNS BREAK !" and communication will be stopped. Also, if the error is occurred, both machines display "TRNS ERROR !" and communication will be sttoped.

NOTE : As diagnostic program area does not have all ASCII code, to display a reception data, some charactor will be changed to other charactor. For example, a chapital letter will be changed to small letter.

Break display (Broken transmission)

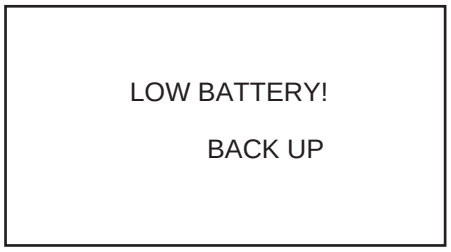


Error display



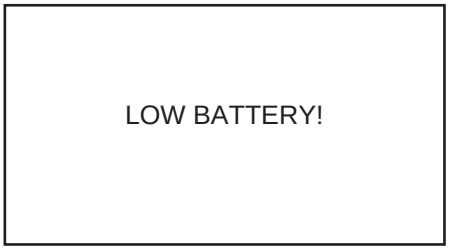
7. Battery level check

Memory back up battery



The memory back up voltage detector detects any irregularity in voltage, the machine goes into an error state and the display is as shown at left figure. To release this display, press any key.

Main battery



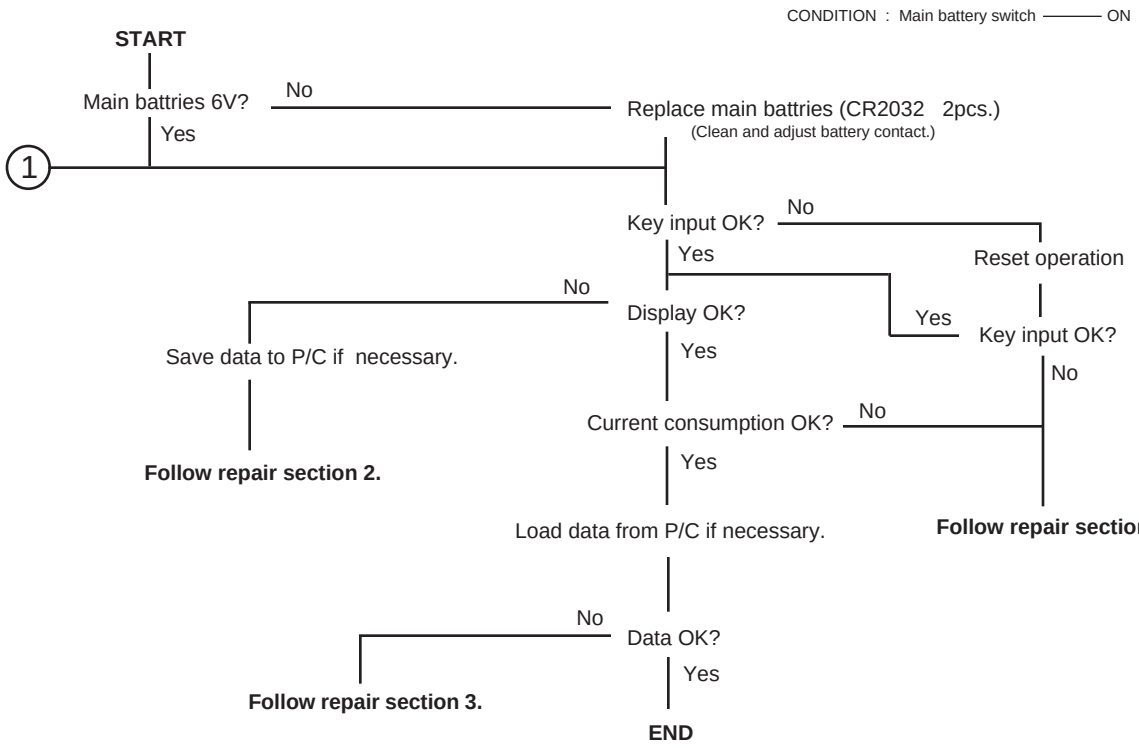
When the main battery voltage detector detects low battery condition while display is on, the machine shows the message as shown at left figure. When this message is displayed, only ON/OFF key are possible to operate. And if the voltage becomes lower than 4.4V, the display will be off mode (auto power off mode).

8. Others

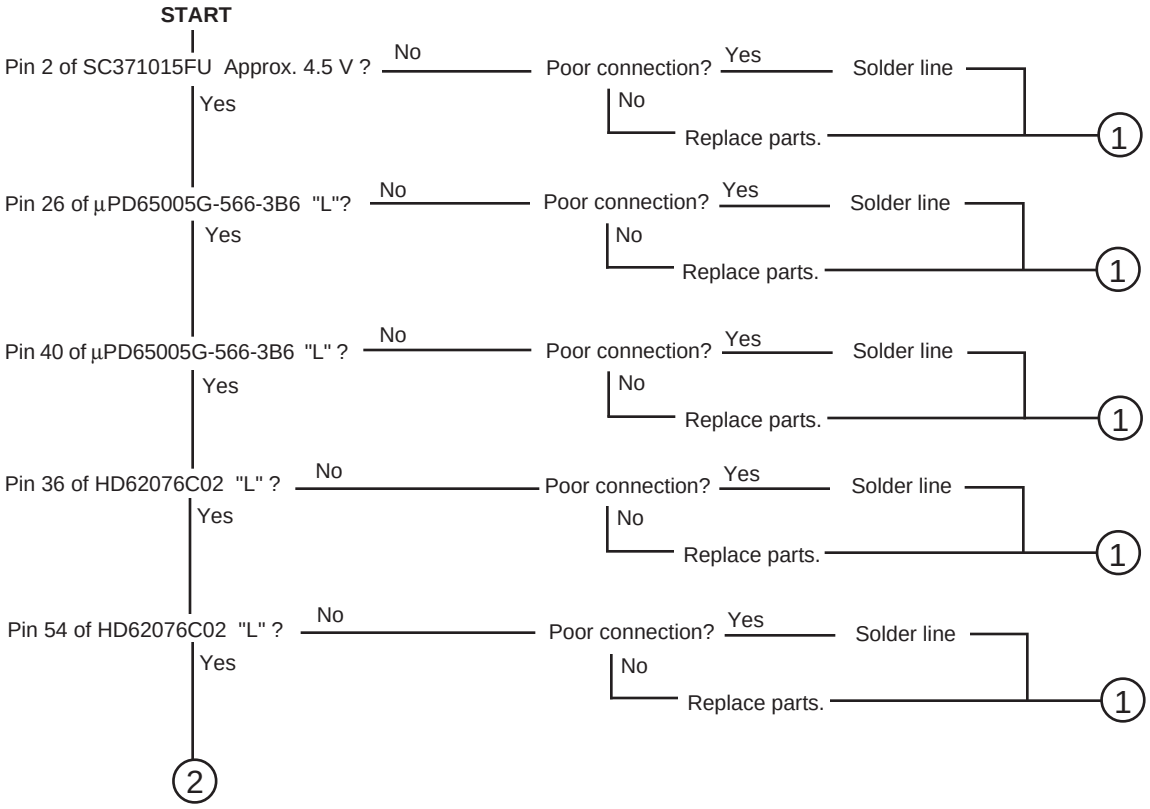
1) When power is off after presetting a alarm time, automatically power is on at a alarm time. However, the display is not reserved in this case.
2) When executing memory sum check, before execute the RAM write check (with SPREADSHEET button).
3) To release diagnostic mode, press reset button.
4) The display contrast can be changed by the contrast volume.

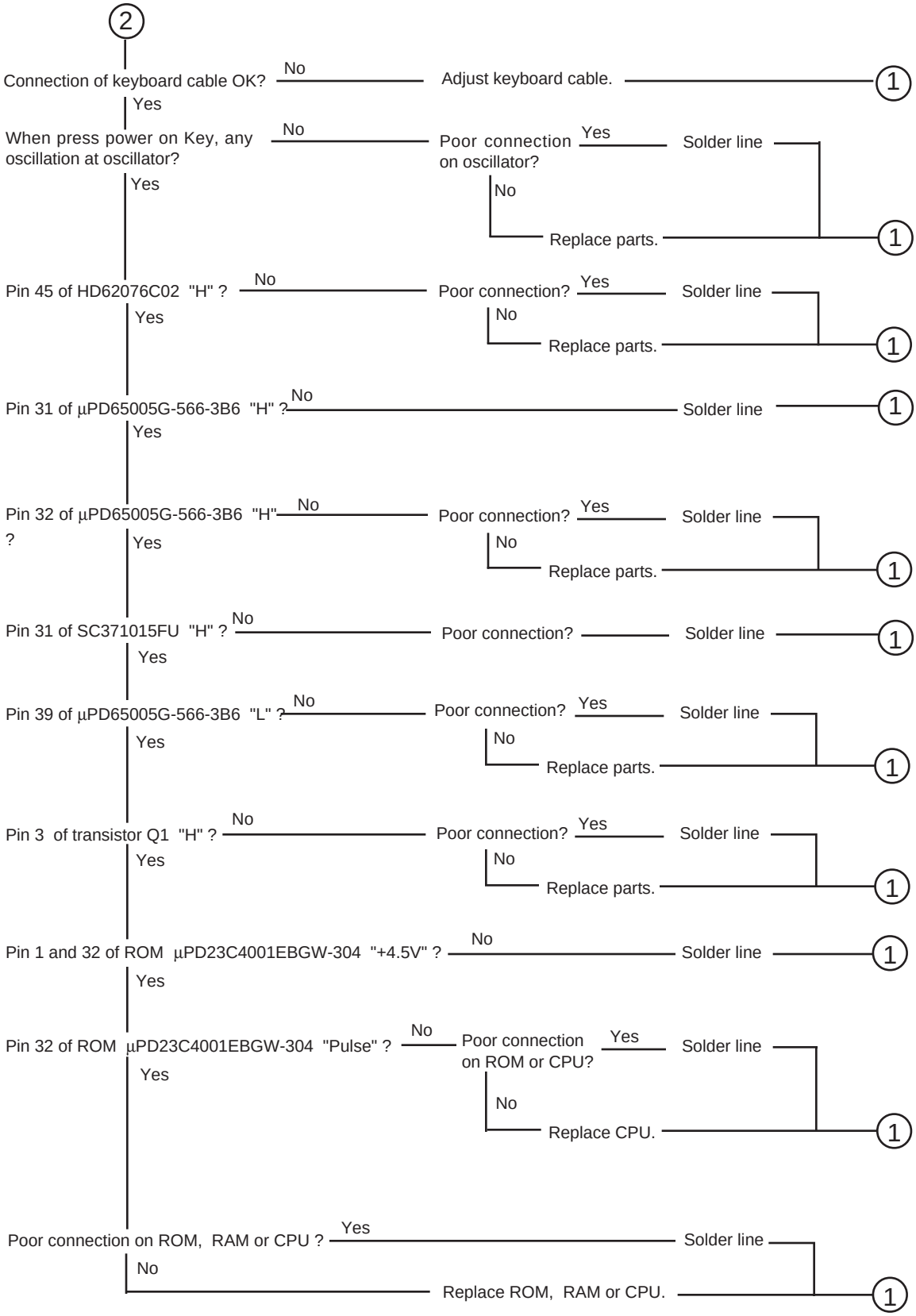
12. TROUBLESHOOTING

Generally, check the machine with the followning steps for repair.

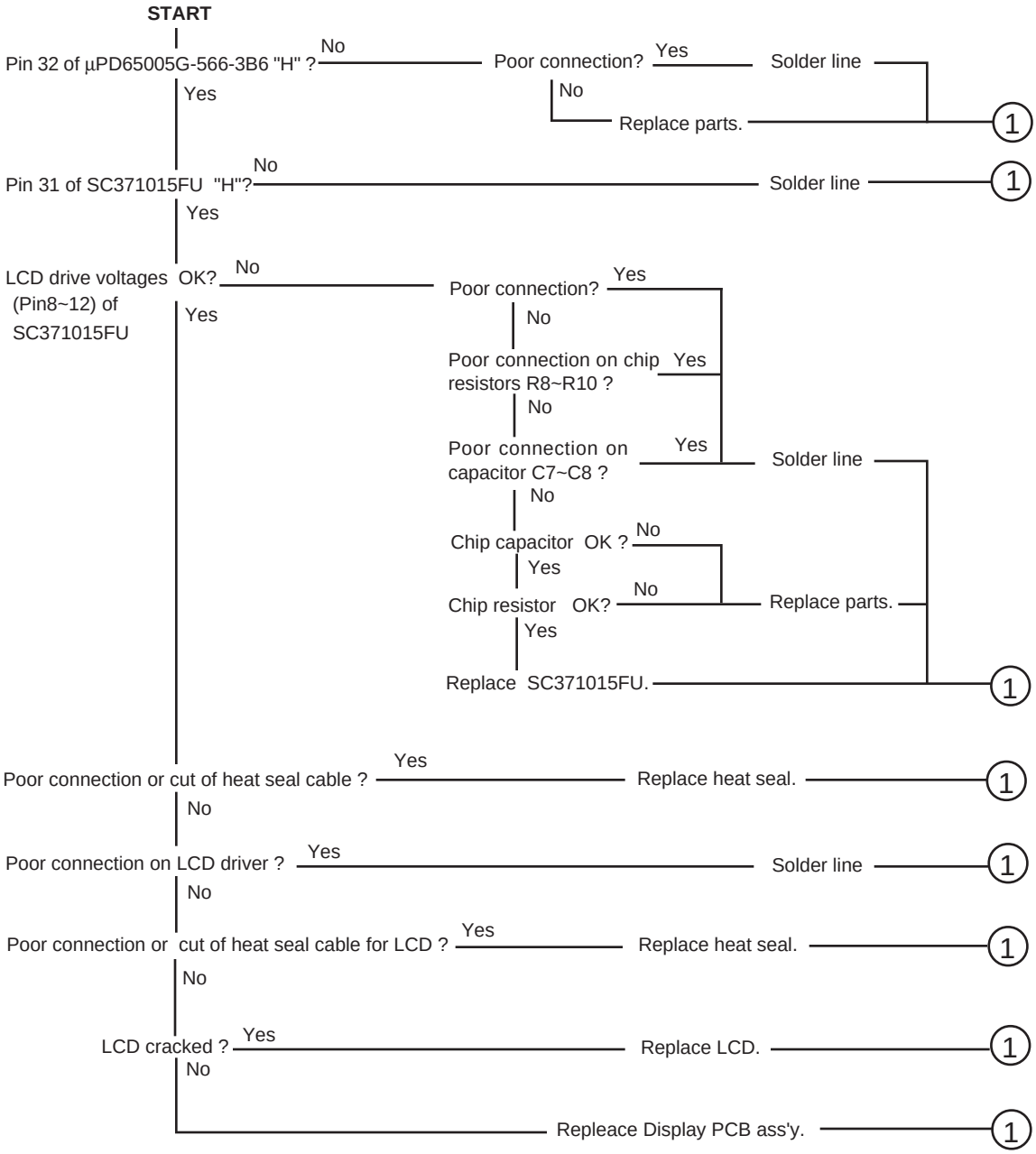


Repair section 1 : For no key input problem

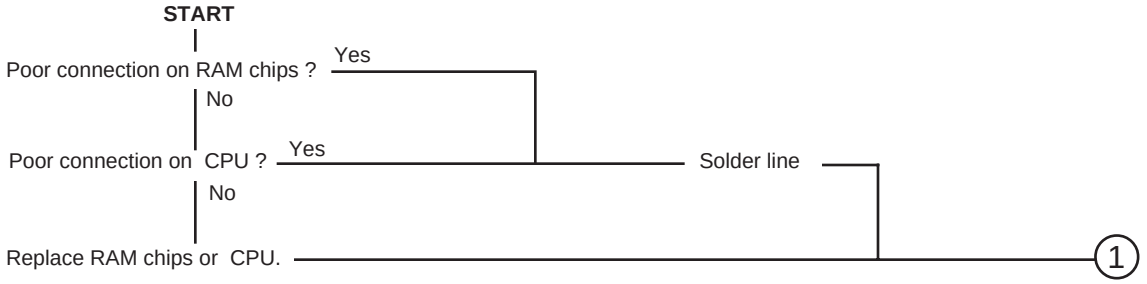



2
Connection of keyboard cable OK?
No
Adjust keyboard cable.
1
Yes
When press power on Key, any oscillation at oscillator?
No
Poor connection on oscillator?
Yes
Solder line
No
Replace parts.
1
Yes
Pin 45 of HD62076C02 "H" ?
No
Poor connection?
Yes
Solder line
No
Replace parts.
1
Yes
Pin 31 of µPD65005G-566-3B6 "H" ?
No
Solder line
1
Yes
Pin 32 of µPD65005G-566-3B6 "H" ?
No
Poor connection?
Yes
Solder line
No
Replace parts.
1
Yes
Pin 31 of SC371015FU "H" ?
No
Poor connection?
Solder line
1
Yes
Pin 39 of µPD65005G-566-3B6 "L" ?
No
Poor connection?
Yes
Solder line
No
Replace parts.
1
Yes
Pin 3 of transistor Q1 "H" ?
No
Poor connection?
Yes
Solder line
No
Replace parts.
1
Yes
Pin 1 and 32 of ROM µPD23C4001EBGW-304 "+4.5V" ?
No
Solder line
1
Yes
Pin 32 of ROM µPD23C4001EBGW-304 "Pulse" ?
No
Poor connection on ROM or CPU?
Yes
Solder line
No
Replace CPU.
1
Yes
Poor connection on ROM, RAM or CPU ?
Yes
Solder line
No
Replace ROM, RAM or CPU.
1

Repair section 2 : For no display or wrong display problem



Repair section 3 : For memory problem



13. PARTS LIST (SF-8500)

N	Item	Code No.	Parts Name	Specification	Q'ty A	Q'ty B	M	FOB Japan N.R.Yen Unit Price	R
		1.CPU BOARD							
N	LSI1	2011 6286	LSI(CPU)	HD62076C02	1	1			A
	LSI2	2105 2422	C MOS IC	SC371015FU	1	1			B
	LSI3	2011 4333	LSI	uPD65005GC-566-3B6	1	1			A
	LSI4	2010 8113	LSI	HD62063B01	1	1			A
N	LSI5	2011 6300	LSI	M5M51008AFP-10LL	1	1			A
N	LSI6	2011 6293	LSI	uPD23C4001EBGW-304	1	1			A
	IC1	2105 1561	C MOS IC	TC7S04F-TE85R	1	1	20		B
	Q1	2250 0546	Chip transistor	2SA1411-T1B(M6)	1	1	20		B
	Q2	2259 0959	Chip digital transistor	DTC114YKT-146	1	1	20		B
	D1	2390 1197	Schottky diode	MA743-(TX)	1	1	10		B
	D2	2390 0364	Schottky diode	MA713-TX	1	1	10		B
	R1,20	2795 3346	Chip resistor	MCR03EZHJ105	2	2	20		C
N	R2	6407 5510	Chip resistor	CC2402310T8	1	1	20		C
	R3,8,9,10,19	2795 3360	Chip resistor	MCR03EZHJ000	5	5	20		C
	R4	2795 3374	Chip resistor	MCR03EZHJ154	1	1	20		C
	R5	2795 3367	Chip resistor	MCR03EZHJ224	1	1	20		C
	R6,11,12	2795 2926	Chip resistor	MCR03EZHJ101	3	3	20		C
	R13	2795 2940	Chip resistor	MCR03EZHJ102	1	1	20		C
	R14	2795 2947	Chip resistor	MCR03EZHJ182	1	1	20		C
	R15	2795 3003	Chip resistor	MCR03EZHJ473	1	1	20		C
	R16	2797 3003	Chip resistor	ERJ-3GEYG164V	1	1			C
	R17,22	2795 3017	Chip resistor	MCR03EZHJ104	2	2	20		C
	R18	2795 3885	Chip resistor	MCR03EZHG103	1	1			C
	C1	2845 2289	Chip capacitor	MCH215C471KK	1	1	20		C
	C2	2845 0427	Chip capacitor	T1-C3K21N1ER221K	1	1	20		C
	C5	2845 2030	Chip capacitor	MCH215C102KK	1	1	20		C
	C6,7	2845 1652	Chip capacitor	MCH215A180JK	2	2	20		C
	C9,10	2845 2499	Chip capacitor	MCH215A300JK	2	2	20		C
	C11	2845 1925	Chip capacitor	MCH312F105ZP	1	1	20		C
	C12	2845 3486	Chip capacitor	MCH312F474ZP	1	1	20		C
	C14,15,16 CB1~3,5	2845 1540	Chip capacitor	MCH212F104ZK	7	7	20		C
	C3	2895 1197	Tantalum capacitor	ECST1AY335R	1	1	20		C
	C8	2895 1204	Tantalum capacitor	ECST0JY106R	1	1	20		C
	C13	2895 1190	Tantalum capacitor	ECST1AX106R	1	1	10		C
	X1	2590 0777	Ceramic oscillator	CSA2.01MGCM001-TC	1	1	5		B
	X2	7110 0642	Crystal oscillator	DT-26S	1	1	10		B
	1	2765 1001	Volume	RK09G-J11TS-100KB	1	1	5		C
N	EF1	3122 2100	Chip EMI	HF50ACB453215-T	1	1	10		C
	2	3501 6405	Miniature jack	HSJ1169-012010	1	1	5		X
N	4	6407 3200	CPU board ass'y (Consists of the above parts)	DB04BX3100T*1	1	1			A
		2.DISPLAY BOARD							
	LSI8~10	2011 1974	TAB LSI	MSM6385AV-Z-358B	3	3			A
N	24	3335 4263	LCD	CD760-TS	1	1			A
	25	6511 7710	Heat seal	FX200P40013	1	1			A
	26	6511 9030	Cushion	FH100024206	2	2			X
	27		Not used						
N	28	6407 3210	D/D board ass'y	APDB04BX01N	1	1			A
		3.COMPONENT							
	3	6511 7270	Insulation plate	ELBDB041106	1	1	20		X
	5	6511 7420	Heat seal	FX201P20172	1	1	5		A

M – Minimum order/supply quantity
R – Rank
Q – Quantity used per unit

A : Except USA, Canada
B : BOSS (for USA, Canada)

N	Item	Code No.	Parts Name	Specification	Q'ty		M	FOB Japan N.R.Yen Unit Price	R
					A	B			
	6	6512 3150	Insulation seal	HGFC0007905	2	2			X
	7	6511 9000	Upper case (DIS)	FAADB040021	1	1			X
	8	6512 3160	Upper case (KB)	FAADB040039	1	1			X
	9	6511 7340	Hinge A	FC002800001	1	1			X
	10	6511 7130	Hinge B	FC002800109	1	1			X
	11	6511 7350	Shaft L	FC000510014	2	2			X
	12	6511 7360	Shaft	FC000510022	2	2			X
N	13	6407 5410	Display plate	EL5G0001106	1	0	1		C
N	14	6407 5440	Display plate for BOSS	EL5G0001203	0	1	1		C
N	15	6407 5420	Upper sheet (DIS)	EL5G0002102	1	1	5		B
N	16	6407 5430	Upper sheet (KB)	EL5G0003109	1	1	5		X
N	17	6407 5450	LCD tape	HGG00011305	1	1	1		X
	18	6511 7140	Key contact rubber A	LADB0420007	1	1			C
	19	6511 7150	Key contact rubber B	LADB0410001	1	1			C
	20	6511 8400	Key contact rubber C	LADB0220105	1	1			C
N	21	6407 5460	Key top set (DIS)	KGDB0410048	1	1	5		C
N	22	6407 5470	Key top set (KB)	KGDB0410056	1	1	1		C
	23	6511 7280	Blind tape	HGFC0005406	1	1			B
N	29	6407 5390	Lower case (DIS)	FABDB040124	1	0	1		X
N	30	6407 5400	Lower case for BOSS (DIS)	FABDB040159	0	1	1		X
N	31	6407 5490	Lower case (KB)	FABDB040141	1	0	1		X
N	32	6407 5480	Lower case for BOSS (KB)	FABDB040132	0	1	1		X
	33	6510 4420	battery insulation tape	HGFC0001109	3	3			X
	34	6402 4700	Nut	MD100000505	2	2			X
	35	6511 7380	Battery spring (+)	EF01DB04000	3	3			X
	36	6511 7390	Battery spring (-)	EF02DB04002	3	3			X
	37	6402 4590	Nut brind	HGFC0002601	2	2			X
	38	6511 7770	Battery cover label	HGFC0004400	1	1			X
	39	6511 7180	Battery holder S	ECDB0411111	1	1			X
	40	6510 4310	Screw (for battery holder S)	MAA80006311	1	1			B
	41	6511 8930	Screw (for hinge)	MAB10033307	2	2			B
	42	6511 7210	Screw	MAB10023301	8	8			B
	43	6511 7220	Screw	MAB10013209	5	5			B
	44	6511 8410	Screw	MAB10015201	2	2			B
	45	6511 7240	Screw	MAA20092300	1	1			B
	46	6510 5250	Screw	MAB80004209	2	2			B
	47		Not used						
	48	6511 7190	Battery holder L	ECDB0411102	1	1			X
	49	6512 0660	Switch knob	FB1DB020500	1	1			C
	50	6406 6250	Switch spring	EF07DB02119	1	1			C
	51	3122 1085	Buzzer	EFB-S45C01AP3	1	1			X
	52	6510 4500	Buzzer tape	HGFC0000501	1	1			X
	53	6511 7080	Knob	FB3DB04008	1	1			X
	54	6511 7160	RB Insert	LC120000102	1	1			C
	55	6511 7290	Battery change label A	HGFC0004604	1	1			X
	56	6511 7300	Battery change label B	HGFC00004701	1	1			X
	57	6511 7780	Battery cover	FADDB040007	1	1			C

M – Minimum order/supply quantity
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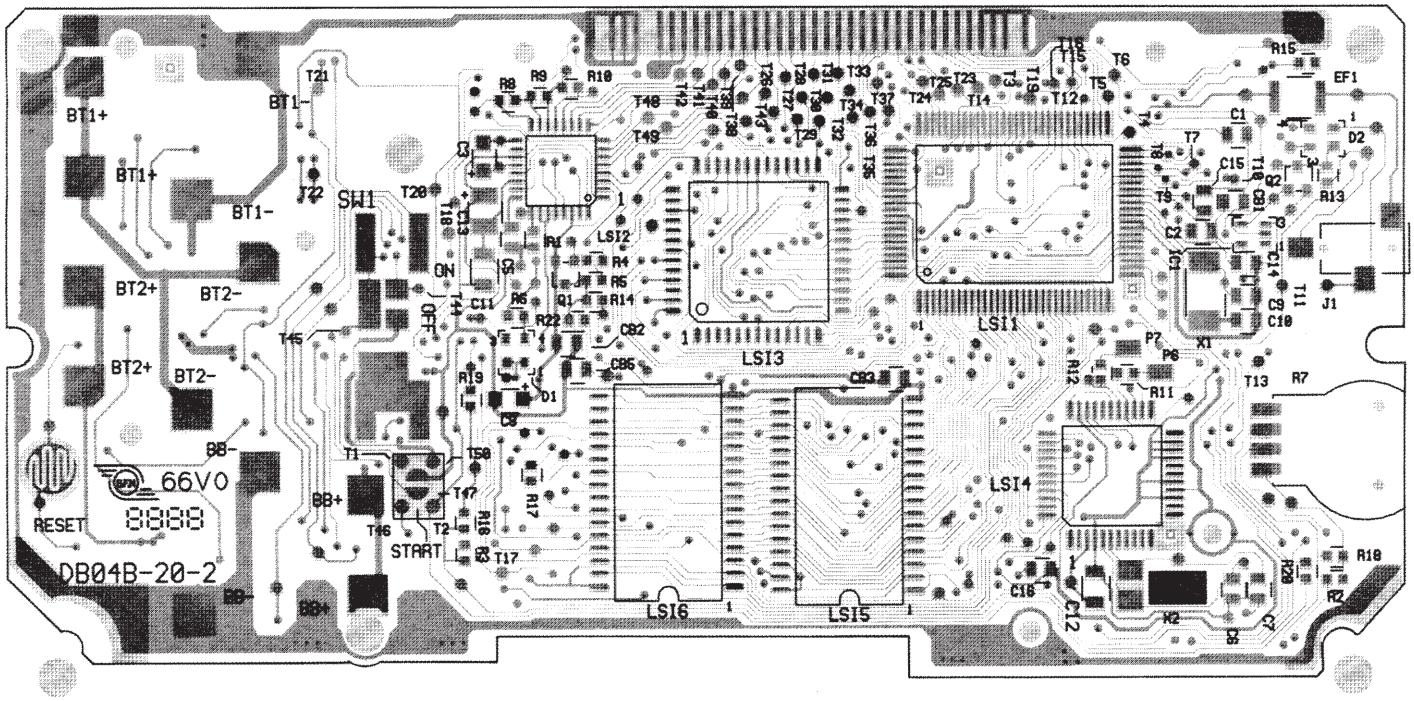
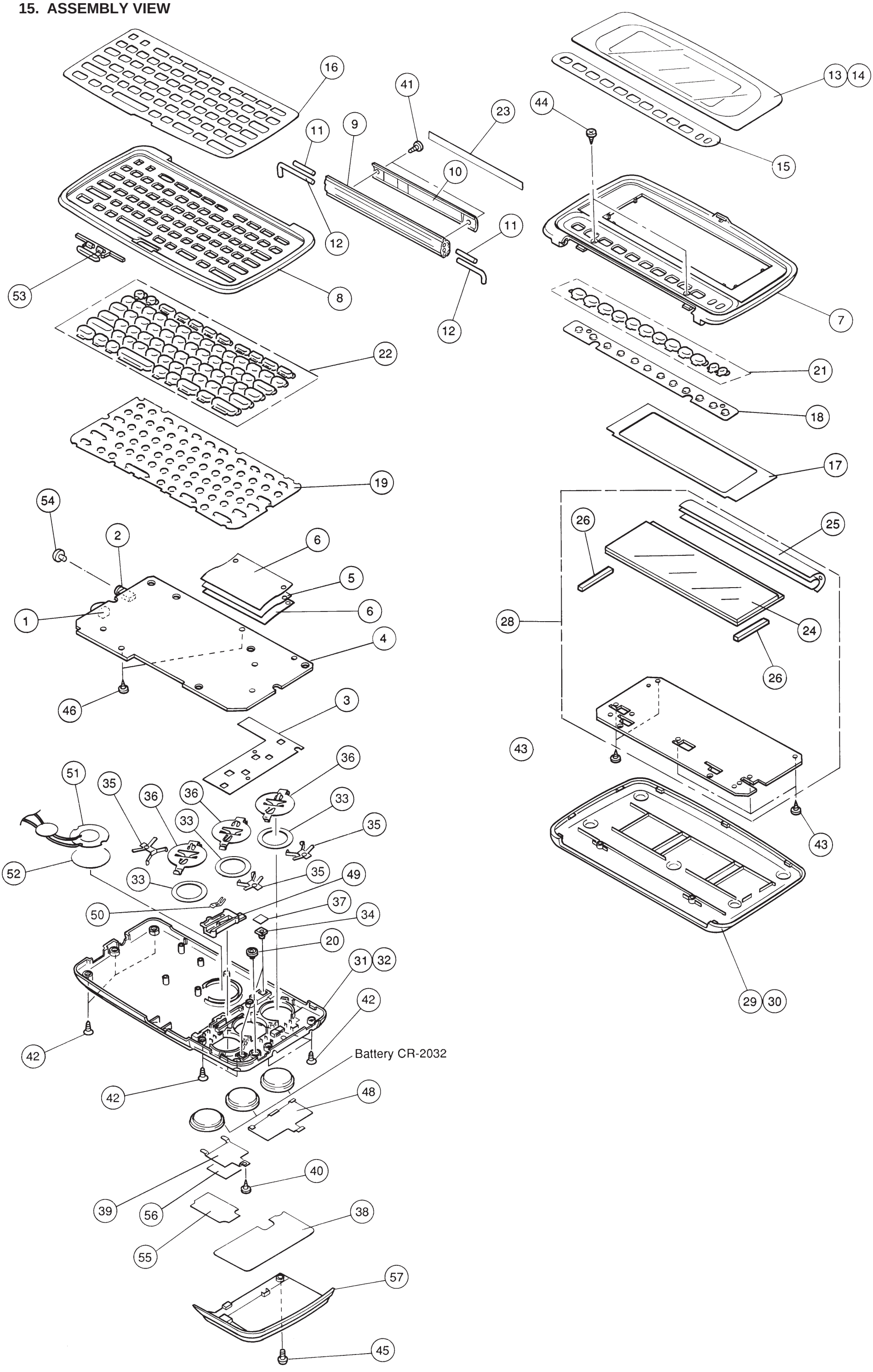
14. PCB VIEW


BT1+
BT1-
BT1+
BT1-
BT2+
BT2-
BT2+
BT2-
BB-
BB+
BB-
BB+
SW1
ON
OFF
START
RESET
66V0
8888
DB04B-20-2
LSI1
LSI2
LSI3
LSI4
LSI5
LSI6
EF1
J1
J2
X1

15. ASSEMBLY VIEW



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